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Bodo´s Power Systems®

Electronics in Motion and Conversion

July 2024

Revolutionizing Circuit Protection with SiC JFETs

The ultra-low $R_{DS(on)}$ and robustness of a JFET paired with the high-voltage capability of silicon carbide – the formidable combination catalyzing semiconductor circuit-breaker development.

qorvo®
all around you

PULSED INDUCTANCE MEASUREMENT

POWER CHOKE TESTER DPG10/20 SERIES WITH 3-PHASE EXTENSION UNIT

Inductance measurement on 1~ and 3~ reactors from 0.1 A to 10 kA

3-PHASE EXTENSION UNIT

- Easy and quick measurement of 3-phase inductors
- Automatic measurement of all windings without reconnecting the terminals
- The software considers the different magnetic flux conditions in the core with 3-phase sinusoidal currents and corrects the measurement results
- The measurement result is equivalent to a conventional measurement with 3-phase sinusoidal mains voltage

KEY BENEFITS

- Very **easy and fast** measurement
- **Lightweight, small and affordable price-point** despite of the high measuring current up to 10000A
- **High sample rate and very wide pulse width range** => suitable for all core materials

APPLICATIONS

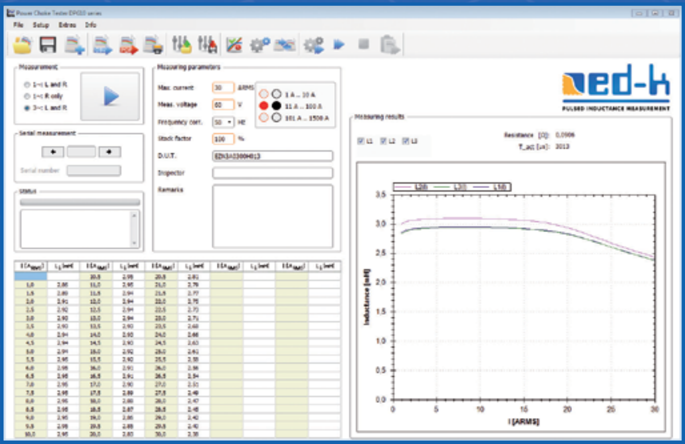
Suitable for all inductive components from **small SMD inductors** to **very large power reactors in the MVA range**

- **Development, research** and **quality inspection**
- **Routine tests** of small batch series and mass production

KEY FEATURES OF THE DPG10/20 SERIES

Measurement of the

- **Incremental inductance** $L_{inc}(i)$ and $L_{inc}(\int Udt)$
- **Secant inductance** $L_{sec}(i)$ and $L_{sec}(\int Udt)$
- **Flux linkage** ψ(i)
- **Magnetic co-energy** $W_{co}(i)$
- **Flux density** B(i)
- **DC resistance**



○ 1~: L and R
○ 1~: R only
● 3~: L and R

Max. current: 30 ARMS
Meas. voltage: 60 V
Frequency corr.: 50 Hz
Stack factor: 100 %
D.U.T.:
Inspector:
Remarks:

○ 1 A ... 10 A
● 11 A ... 100 A
○ 101 A ... 1500 A

Technological leader in pulsed inductance measurement for 18 years

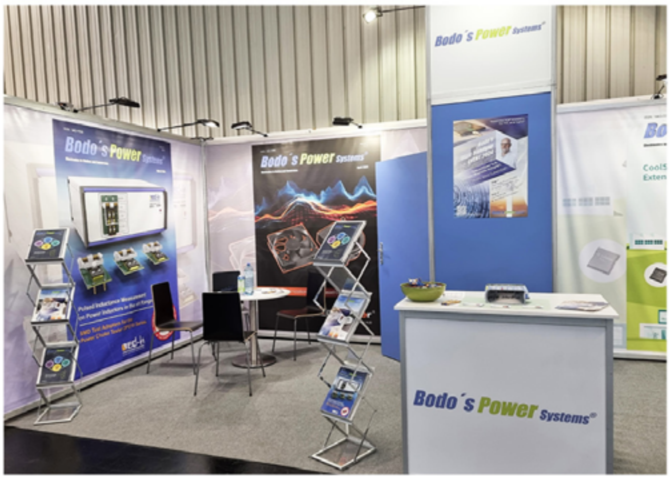
www.ed-k.de

EC
MP88
.22 +/-10%
1600VDC

Content


Technology Stage
7A


#PCIMEUROPE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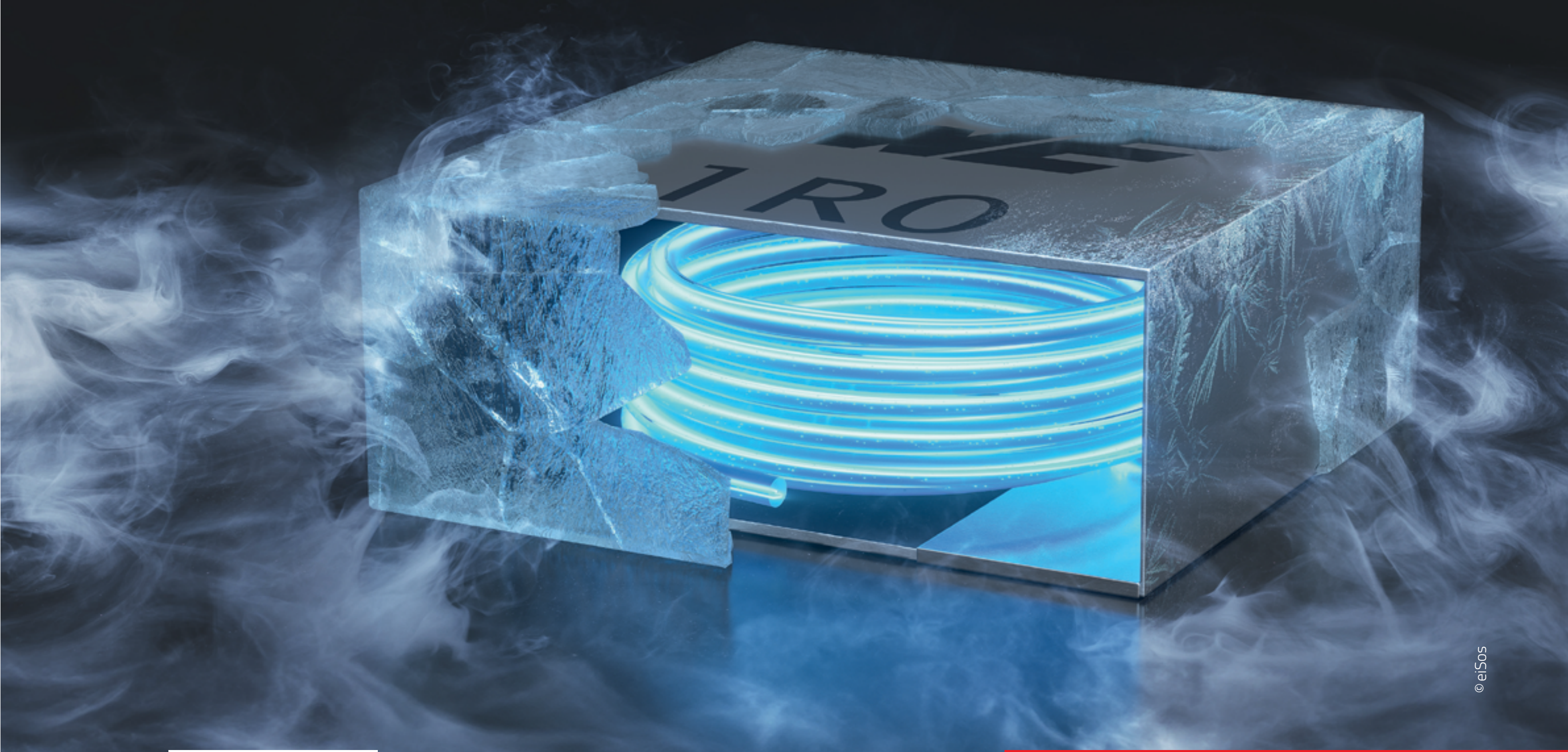

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The Significance of Power

In the beginning was the fire, and it enabled mankind to become more and more independent of the elements on earth. Without fire, mankind would have neither been able to settle in colder regions of our planet nor to expand its entire population beyond a few million inhabitants worldwide. Fire enabled steam engines and the industrialization, and the “fire of the information age” is data – enabled through electricity powering server farms. So far, electricity is the most convenient form of energy as it allows for easy transformation into heat and cold, movement, light etc. By the way: About 1.4 billion people do not have access to electricity – today!

Considering this, we understand why we gave the practical use of electricity the name “power”. The daily use of electricity has become so ubiquitous and omnipresent that we just “supply power” like we supply food or water. Electrical power has become the lifeblood of our modern society, and this is the reason why power supplies and power systems are such an important utility.

Here at Bodo’s Power Systems, we permanently aim to make your life as a power system designer easier and more effective. This is the reason why our entire team went to PCIM in Nuremberg to get the latest updates as well as to welcome you to our booth. Our editorial team (Bodo, Holger and myself) spoke with many industry experts, and one fact became obvious: the era of wide bandgap semiconductors has only just begun in all kinds of power applications. This was very impressively shown at the wide bandgap presentation session on PCIM’s Technology Stage, where you had to be early to get a seat and several people had to listen standing. This session, which was solely organized by Bodo’s Power Systems, comprised of two 1-hour sessions discussing SiC and one session on GaN. But this was just a foretaste of Bodo’s Wide Bandgap Event, where you will be able to immerse yourself more intensively in the world of SiC and GaN on December 3 and 4 at the Munich Airport Hilton.

Bodo’s magazine is delivered by postal service to all places in the world. It is the only magazine that spreads technical information on power electronics globally. We have EETech as a partner serving our clients in North America. If you speak the language, or just want to have a look, don’t miss our Chinese version at bodospowerchina.com. An archive of our magazine with every single issue is available for free at our website bodospower.com.

Green tip of the month: The era of fire is basically over, the era of electricity is here. So, whenever you can afford it, choose your energy supplies in a way that you receive energy from renewable sources only and say good-bye to fire-relating technologies as fast as possible. Our (Grand)children will thank you for it.

Alfred Vollmer

Events

electronica China 2024
Shanghai, Cina July 8 – 10
www.electronicachina.com.cn

SEMICON West 2024
San Francisco, CA, USA July 9 – 11
www.semiconwest.org

PCIM Asia 2024
Shenzhen, China August 28 – 30
www.pcimasia-expo.com

ECCE Europe 2024
Darmstadt, Germany September 2 – 6
www.ecce-europe.org

ESREF 2024
Parma, Italy September 23 – 26
www.esref2024.org

INNOTRANS 2024
Berlin, Germany September 24 – 27
www.innotrans.de

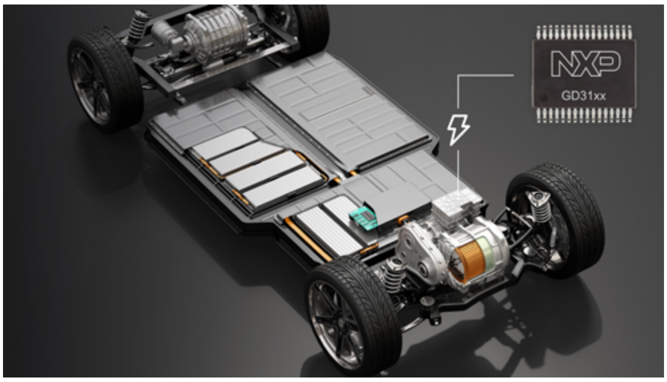
ECCE 2024
Phoenix, AZ, USA October 20 – 24
www.ieee-ecce.org

WiPDA 2024
Dayton, OH, USA November 4 – 6
https://wipda.org

electronica 2024
Munich, Germany November 12 – 15
https://electronica.de

Collaboration on SiC-Based Traction Inverters for Electric Vehicle Powertrains

NXP Semiconductors announced a collaboration with automotive tier-1 ZF Friedrichshafen on SiC-based traction inverter solutions for electric vehicles. Using NXP's GD316x high-voltage (HV) isolated gate drivers, the solutions are designed to accelerate the adoption of 800-V and SiC power devices. Safe, efficient and higher performance traction inverters enabled by the GD316x product family can be designed to extend EV range and reduce the number of charging stops while lowering system level costs for OEMs.



As traction inverters now migrate to SiC-based designs, the SiC power devices need to be paired with HV isolated gate drivers to harness the advantages such as higher switching frequency, lower conduction losses, better thermal characteristics and higher robustness at high voltages, compared to previous generation silicon-based IGBT and MOSFET power switches. The GD316x family of functionally safe, isolated, high voltage gate drivers incorporates a number of programmable control, diagnostic, monitoring, and protection features, enhanced to drive the latest SiC power modules for automotive traction inverter applications. Its high level of integration allows a smaller footprint and simplifies the system design. The capabilities reduce Electromagnetic Compatibility (EMC) noise while also reducing switching energy losses for better efficiency.

www.nxp.com

Opening of Manufacturing Plant in Mexico

Littelfuse held a ribbon-cutting ceremony to celebrate the opening of a new manufacturing plant in Piedras Negras, Coahuila, Mexico. The newly opened and operational 10,000-square-metre facility, which doubles the current local Littelfuse manufacturing capacity while maintaining room for additional expansion, is located close to three other company operations in the city. The facility's innovative automation systems ensure precision and efficiency, allowing for a high degree of customization to meet specific client needs.

The purpose-built facility utilizes water treatment processes resulting in zero water consumption. The smart air compressors, high-efficiency HVAC, safety relays, and use of LED lighting throughout the facility deliver energy effectively and efficiently. The manufacturing operations team of 1,000 employees is being staffed from a combination of current talent from nearby Littelfuse locations and new hires. The facility is fully accessible, convenient to public transportation and daycare, and will bring increased opportunities for career development and community outreach and support.

www.littelfuse.com

Support for 300mm Smart Power Process

In a joint development project spanning around one year, important progress was made in the production of “Smart power technologies”. Fraunhofer IPMS provided significant support to the semiconductor manufacturer Infineon by supplying selected process modules within the entire CMOS process value chain on 300 mm wafers. The collaboration played a key role in the process development for the factory expansion at Infineon Dresden. Over 2000 wafers were successfully processed as part of this collaboration. The wafers were exchanged several times between Fraunhofer IPMS and Infineon Dresden to ensure optimal use of resources and optimum integration into the production lines.

The teams are now well attuned to each other. The cooperation was always focused on achieving results, and the colleagues at Infineon were very accommodating towards Fraunhofer's ideas. With the construction of the new Smart Power Fab, Infineon is making one of the largest single investments in its history. The aim of the semiconductor manufacturer is to increase the speed at which it expands its semiconductor production capacities and to further strengthen Europe as a chip manufacturing location. This is an important contribution to meeting the growing global demand for semiconductors - for example for applications to generate renewable energy, for use in data centers and for electromobility.

www.ipms.fraunhofer.de

Tradeshow emphasizes Smart Energy Solutions

electronica 2024

World's leading trade fair and conference for electronics

As electronics is a key factor in the energy transition and development of smart energy solutions, smart energy will be a key topic at electronica 2024, which will take place from November 12 to 15 in Munich, Germany. According to a report by MarketsandMarkets, the global market for smart energy is expected to grow from 170 billion US dollars in 2022 to 283 billion US dollars by 2027, which is equivalent to a compound annual growth rate (CAGR) of 10.6%. The main driver of this growth is the increasing demand for intelligent power grids, known as smart grids.

At electronica 2024, which is all about the all-electric society, the topic of smart energy will play a correspondingly important role, whether at the trade fair stands or in the conference and forum program. The Power Electronics Forum in Hall A5, for example, will look at the entire spectrum of power electronics. Here, experts will discuss current trends and developments that are of crucial importance for the energy transition and for implementing the all-electric society. Hall A4 will be all about innovations in transformers, power supplies, power supply units and batteries. In Halls B4, B5, C3, C4 and C5, numerous exhibitors will be presenting their latest products and solutions relating to semiconductors, while embedded systems can be found in Hall B4.

www.electronica.de

Call for Papers

APEC 2025

ATLANTA, GA | MARCH 16-20

APEC 2025 will take place March 16-20, 2025 at the Georgia World Congress Center in Atlanta, GA, and the Technical Session digest submissions will be opening in a few weeks for APEC 2025. The organizer assures that APEC 2025 will continue the long-standing tradition of addressing issues of immediate and long-term interest to the practicing power electronics engineering community. Outstanding technical content is promised to be provided at one of the lowest registration costs of any IEEE conference. To be considered as a Technical Session paper for APEC 2025, it is advised that the applicant's digest/paper should address the following: The challenge to be addressed by the paper as well as the major results and how this differs from the most relevant existing literature. Papers presented at APEC must be original material and not have been previously presented or published. The principal criteria in selecting digests will be the usefulness of the work to the practicing power electronic professional. Reviewers value evidence of completed experimental work. Authors should obtain any necessary company and governmental clearance prior to submission of digests.

www.apec-conf.org

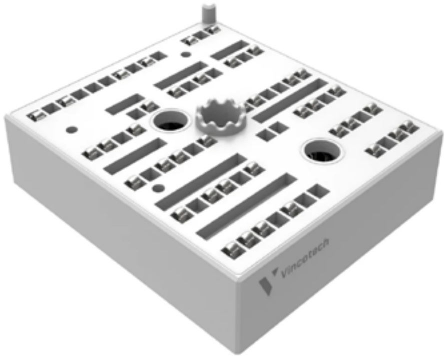
Cooperation to offer SmartSiC

X-FAB and Soitec will begin work to offer Soitec's SmartSiC™ wafers for the production of silicon carbide power devices at X-FAB's plant in Lubbock, Texas. This collaboration follows the successful completion of the assessment phase, during which silicon carbide (SiC) power devices were manufactured at X-FAB Texas on 150mm SmartSiC wafers. Soitec will offer X-FAB's customers easy access to the SmartSiC substrate through a joint supply chain consignment model.

SmartSiC is a proprietary Soitec technology based on the company's SmartCut™ process, in which a thin layer of a high-quality monocrystalline (mono-SiC) 'donor' wafer is split off and bonded to a low resistivity polycrystalline (poly-SiC) 'handle' wafer. The resulting substrate offers improved device performance and manufacturing yields. The process allows multiple re-uses of a single donor wafer, significantly reducing cost and related CO_2 emissions.

www.xfab.com

Renewal of Cooperation Agreement for Packaging Technology



Vincotech has renewed its cooperation agreement with Semikron Danfoss. The two enterprise's alliance, which dates back to 2003, has been extended to further strengthen MiniSKiiP® package technology. Multiple source options for the package to further mitigate the supply chain risk, and standards-compliant design are just a few of the benefits of this renewed cooperation agreement. Featuring service-friendly spring contacts, MiniSKiiP's hardware is in mass production for use in motor drives, servo drives, and power supplies. Vincotech and Semikron Danfoss are now set to take MiniSKiiP's reliability and standardization to the next level. Customers can look forward this tech bringing even greater robustness, versatility, and compatibility for their power electronics solutions.

www.vincotech.com


PASS LINE
FIELD
COME
SIX
8
NINE
10
HORN HIGH
10 FOR 1
5 FOR 1

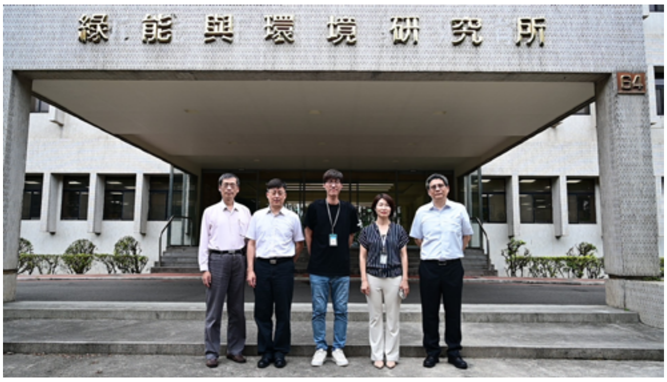
Building Permit for final Construction Phase of Smart Power Fab in Dresden

Infineon Technologies is on schedule with the construction of the Smart Power Fab in Dresden and is initiating the final construction phase. During a visit, the Prime Minister of the Free State of Saxony, Michael Kretschmer, officially handed over the last outstanding building permit for the new fab issued by the State Directorate of Saxony. The excavation of the building pit has now been completed. The shell and building construction are currently progressing on the concrete foundation, which is up to two meters thick. Infineon officially broke ground for the new plant in Dresden in May 2023. Manufacturing is scheduled to start in 2026. With a total investment of five billion euros, the company is making a significant contribution to the European Commission goal to increase the EU's share of global semiconductor production to 20 percent by 2030. Infineon is aiming for public funding of around one billion euros. On average, construction workers have removed around 8,000 tons of soil every day since the start of work. A total of 450,000 cubic meters of excavated soil has been produced, which corresponds to the volume of 180 Olympic swimming pools.

www.infineon.com

MoU for GaN Semiconductors

The fabless semiconductor company Cambridge GaN Devices (CGD) has signed a Memorandum of Understanding (MoU) with Industrial Technology Research Institute (ITRI) of Taiwan to solidify a partnership in developing high performance GaN solutions for USB-PD adaptors. The MoU also covers the sharing of domestic and international market information, joint visits to potential customers and promotion. CGD’s IC-enhanced GaN – ICeGaN™ – is a novel platform that improves ease-of-use, facilitates smart temperature control and enhances gate reliability. The first commercialized product in the market to adopt GaN devices has been USB-PD adaptors, and it is this market that the first designs from the partnership will address. Specifically, the agreement covers the development of power solutions in the 140-240 W range with power densities exceeding 30 W/in^3 for e-mobility, power tools, notebook and cell phone applications.



www.camgandevices.com

SiC Inverter Control Module to drive autonomous vehicle Electric motors

Applied EV, a leader in vehicle control system technologies for Software Defined Machines™, announced they have selected CISSOID's CXT-ICM3SA series of Silicon Carbide Inverter Control Modules (ICMs) to drive their latest generation of autonomous vehicle E-motors. Dedicated to the E-mobility market, CISSOID’s software-powered SiC ICMs are augmented with onboard programmable hardware, accelerating the response time to critical events, off-loading the processor cores and enhancing functional safety.

The ICM is integrated into Applied EV’s Digital Backbone™, a centralised control system combining software and hardware, setting a new benchmark for safety rated vehicles. Applied EV’s CEO, Julian Broadbent, said “Both Applied EV and CISSOID recognise functional safety is critical in the development and deployment of autonomous vehicles. The partnership integrates CISSOID’s ICMs into our Digital Backbone, allowing for a faster development cycle, giving our customer the safest vehicle in the shortest time possible.”

CISSOID’s CEO, Dave Hutton, said: "We are excited to embark on this collaborative journey with Applied EV to drive innovation in e-mobility. By combining our expertise in electric motor design with Applied EV’s proficiency in software and vehicle integration, the aim is to deliver a game-changing electric motor drive platform for the future of mobility together."

The collaboration underscores the shared commitment to driving positive change in the automotive industry and contributing to a more sustainable future for transportation globally.

www.cissoid.com

The 7th Generation Modules

Dual XT, Premium Dual XT & Dual XT RC-IGBT

series
7G

DualXT – Main features

- 7G IGBT & FWD
- New internal layout
- Higher reliability
- Improved silicone gel
- Solder or mini press-fit pins
- More power, lower losses

Premium DualXT – Additional features

- Advanced bond wire design
- High thermal conductive ceramic substrate
- Package material with CTI > 600
- $V_{iso} = 4$ kV
- High power density

Dual XT Reverse Conducting IGBT

- RC-IGBT integrates IGBT and FWD functions into a single chip
- This technology leads to further miniaturization
- Increase of power density
- Extended chip area leads to a chip temperature reduction by lower $R_{th(j-c)}$
- Benefits in thermal behavior of the chip and module
- Three times higher i^2tcapability

www.fujielectric-europe.com

Fuji Electric
Innovating Energy Technology

Preferred Partner of Semiconductor Manufacturer

Würth Elektronik is now a preferred partner at Renesas. By partnering with Renesas as a preferred partner, Würth Elektronik gains access to a host of resources and support to further enhance its capabilities in delivering innovative solutions, as well as joint solution options shown at tradeshows, webinars, seminars, and blog articles. This partnership also signifies Würth Elektronik's dedication to reducing development risks and accelerating time-to-market for customers by leveraging Renesas' extensive portfolio of products and solutions. Renesas preferred partners are elite system solution providers renowned for their expertise in deploying Renesas products to deliver highly optimized solutions. These partners undergo rigorous training and boast extensive experience, ensuring they can effectively leverage Renesas technologies to meet diverse customer needs. Renesas' preferred partners play a crucial role in bringing value-added solutions to customers, whether in the early stages of prototyping, sample and technical support, or advancing towards productization based on proof of concepts (PoCs) from Renesas or its partners. This collaboration ensures that customers benefit from optimized solutions that meet the relevant standards of quality and performance.

www.we-online.com

The first fully integrated SiC Facility in Italy

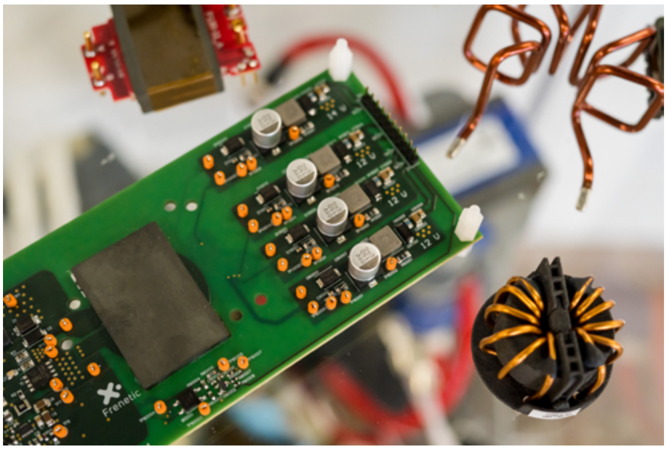
STMicroelectronics intends to build a high-volume 200mm silicon carbide manufacturing facility for power devices and modules, as well as test and packaging, to be built in Catania, Italy. Combined with the SiC substrate manufacturing facility being readied on the same site, these facilities will form ST's Silicon Carbide Campus. The Silicon Carbide Campus will serve as the center of ST's global SiC ecosystem, integrating all steps in the production flow, including SiC substrate development, epitaxial growth processes, 200mm front-end wafer fabrication and module back-end assembly, as well as process R&D, product design, advanced R&D labs for dies, power systems and modules, and full packaging capabilities. This will achieve a first of a kind in Europe for the mass production of 200 mm SiC wafers with each step of the process – substrate, epitaxy & front-end, and back-end – using 200 mm technologies for enhanced yields and performances.

The facility is targeted to start production in 2026 and to ramp to full capacity by 2033, with up to 15,000 wafers per week at full build-out. The total investment is expected to be around five billion euros, with a support of around two billion euros provided by the State of Italy within the framework of the EU Chips Act.

www.st.com

Online Custom Magnetics Design House launches global Production Service

Frenetic Electronics announced Frenetic Factory, a worldwide magnetics production facility with plants in the USA, Mexico, Europe, India, and China. Frenetic Factory can deliver samples quickly with no MOQs. It currently has a production capacity of 8.75M units annually, that can be scaled to even higher volumes fast. Frenetic launched its magnetics design service in 2021. Using an online process and Core Optimizer tool to make the core selection process faster and more efficient, users input their electrical and environmental specifications, and receive an optimized transformer design in minutes by using Frenetic's custom algorithms. The company's web-based platform allows users to compare millions of different magnetics possibilities within seconds. BOMs, 3D models and engineering drawings are automatically generated. Now, users can take that design and have samples and full production quantities made at Frenetic Factory. Frenetic Factory comprises facilities around the world that are both owned by Frenetic Magnetics or a qualified third party. This is the same operational model as much of the rest of the electronic components industry. And Frenetic Factory is fully responsible for the technical support and quality of the components it supplies, no matter which facility they were produced in.



Manufacturing quality and product standards adhered to include MIL-STD-461E, MIL-STD-981, ESCC 3201 and Qualified Parts, and AEC-Q200.

www.frenetic.ai


HIOKI
CT6877A
AC/DC CURRENT SENSOR
2000A
HIOKI VT1005 AC/DC HIGH VOLTAGE DIVIDER
PW8001 POWER ANALYZER
CT6872 AC/DC CURRENT SENSOR
50A
HIOKI CT6841A AC/DC CURRENT PROBE
20A

GaN Power Transistors Addressing a Broad Range of Applications

Ultra-high power density and efficiency beyond Titanium level: CoolGaN™ Transistor 700 V G4

Infineon’s new CoolGaN™ Transistor 700 V G4 family achieves higher levels of efficiency and power density with excellent figures of merit (FOM) delivering outstanding switching and conduction-loss performance with high cost-effectiveness.

Power supply designs with CoolGaN™ Transistors 700 V G4 exceed the new OCP M-CRPS performance standards. They also achieve higher light-load efficiencies – critical for data center sustainability requirements – resulting in more savings on total system costs. With these products, 3.2 kW power supplies that reached 100 W/in^3 in 2022 now have efficiencies higher than the Titanium level, reaching 120 W/in^3 and above.

Part number	Typ. $R_{DS(on)}$	Package dimensions
GS-065-030-6-LL	40 mΩ	TOLL (9.9 x 10.375 x 2.3 mm)
GS-065-030-6-LR	37 mΩ	PDFN8x8 (8.0 x 8.0 x 0.9 mm)
GS-065-018-6-LR	62 mΩ	PDFN8x8 (8.0 x 8.0 x 0.9 mm)
GS-065-014-6-LR	95 mΩ	PDFN8x8 (8.0 x 8.0 x 0.9 mm)
GS-065-014-6-L	95 mΩ	PDFN5x6 (5.0 x 6.0 x 0.85 mm)
GS-065-011-6-LR	125 mΩ	PDFN8x8 (8.0 x 8.0 x 0.9 mm)
GS-065-011-6-L	125 mΩ	PDFN5x6 (5.0 x 6.0 x 0.85 mm)
GS-065-008-6-L	165 mΩ	PDFN5x6 (5.0 x 6.0 x 0.85 mm)
GS-065-004-6-L	315 mΩ	PDFN5x6 (5.0 x 6.0 x 0.85 mm)

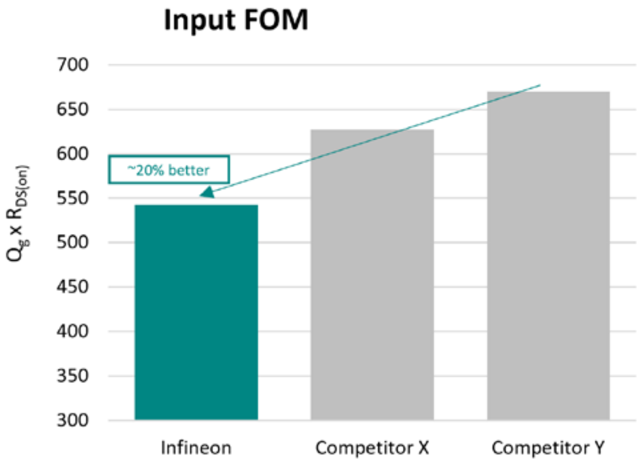
Table 1: CoolGaN™ Transistors 700 V G4

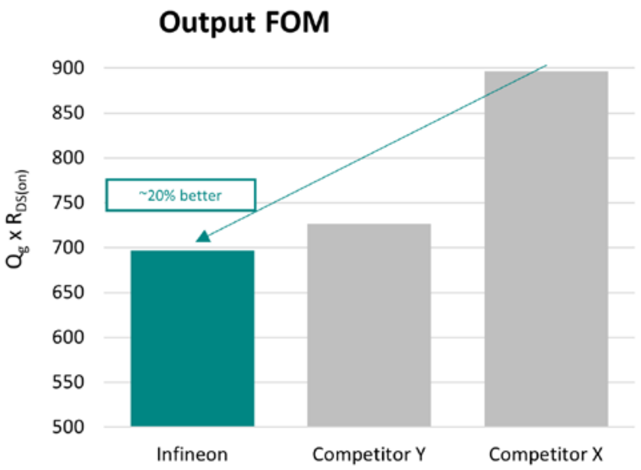
CoolGaN™ Transistor 700 V G4 family feature >20 percent improvements in input and output FOMs, meaning reduced losses, enhanced efficiency, and more cost-effective solutions. The new family has an increased device-specification granularity and comes in various packages (Table 1). Thus, package combinations to optimize electrical and thermal system performance with the correct $R_{DS(on)}$ resistance for power systems from 20 W to 25 kW are possible. Infineon now provides 700 V e-mode products with an outstanding 850 V transient voltage rating, significantly enhancing system reliability and robustness, enabling other components to withstand anomalies such as voltage spikes, ensuring uninterrupted and dependable performance.

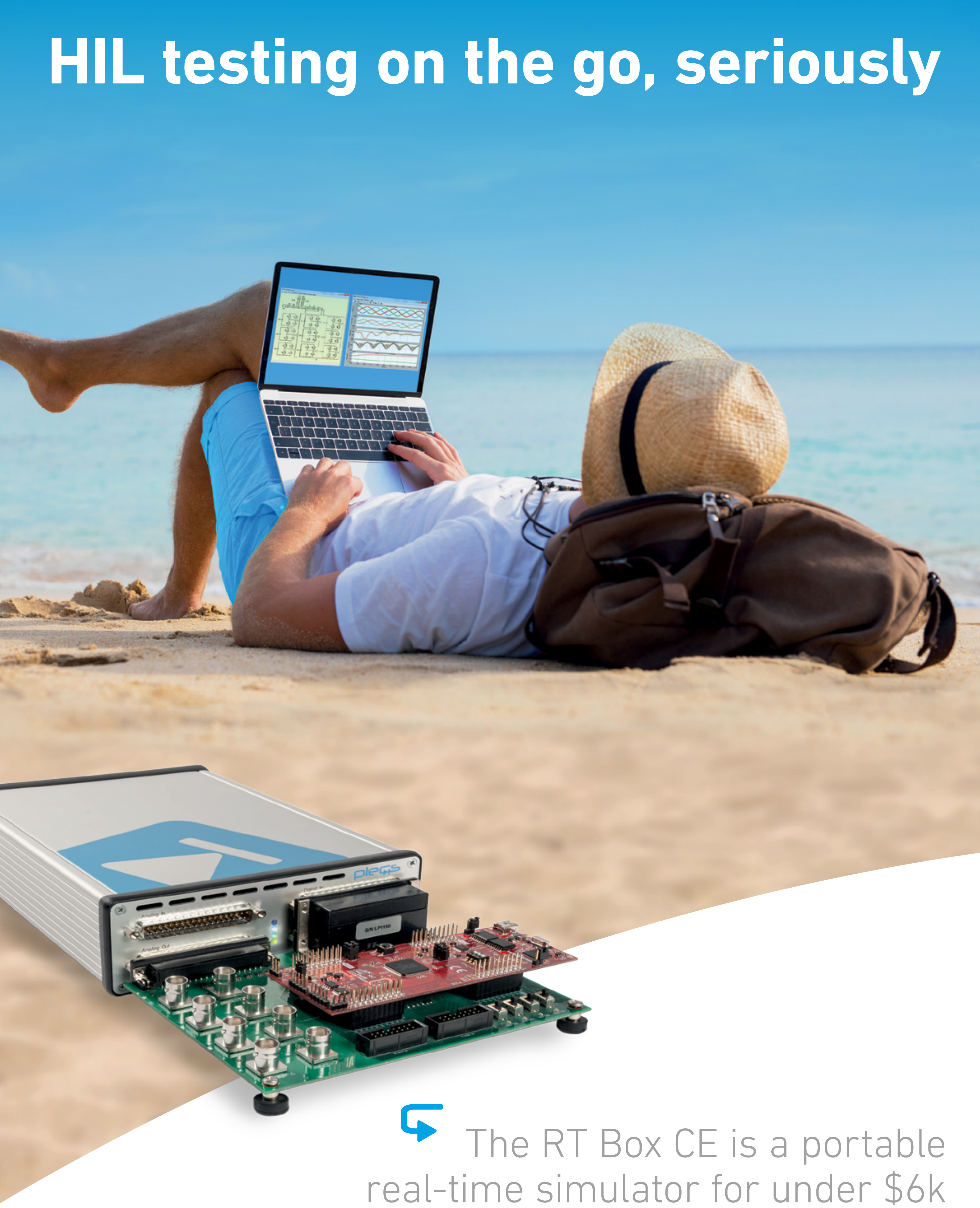
The CoolGaN™ Transistor 700 V G4 portfolio consists of 13 products with $R_{DS(on)}$ range from 20 mΩ to 315 mΩ, available in standard 5x6 and 8x8 PDFN, TOLL, and TOLT packages. Products available to order immediately are listed in Table 1. Scan the QR code to browse the portfolio online.

Click here to browse portfolio online!

www.infineon.com






HIL testing on the go, seriously
plecs
Analog In
Analog Out
Digital In
S/N LP1150
The RT Box CE is a portable real-time simulator for under $6k
plexim
electrical engineering software

Revolutionizing Circuit Protection with SiC JFETs

The mid-20th century was a time of significant innovation in residential and industrial electrical systems. One of the most impactful advancements was the transition from traditional replaceable fuses to miniature circuit breakers (MCBs). While fuses provided basic protection, they had to be replaced after they blew. Circuit breakers, on the other hand, could be easily reset after tripping. This convenience led to building codes and electrical standards favoring circuit breakers over fuses in new construction.

By Jonathan Dodge, P.E., Principal Applications Engineer,
and Andy Wilson, Senior Business Development, Qorvo

Innovations such as ground fault circuit interrupters (GFCIs) and arc fault circuit interrupters (AFCIs) have further enhanced circuit breakers over the years. Despite these improvements, traditional circuit breakers still have limitations because of their mechanical relays. These **limitations** include:

- **Arcing:** When relay contacts open or close, arcing can occur, which is especially problematic during circuit faults with high currents.
- **Disconnect speed:** The speed at which an electromechanical circuit breaker disconnects is limited by the physics of its coil and the relay's inertial mass.
- **Wear and tear:** Over time, the contacts in a mechanical relay wear out, limiting the number of interruption cycles.

The current trend is moving toward developing a new type of circuit breaker that replaces the electromechanical relay with semiconductor power devices, known as solid-state circuit breakers (SSCBs) or semiconductor circuit breakers (SCBs). These SSCBs offer several **advantages**:

- **Arcing:** Semiconductor switches connect and disconnect without producing arcs, eliminating the need for special arc-suppression features.
- **Disconnect speed:** Free from the constraints of a magnetic coil, semiconductor switches can operate hundreds of times faster than electromechanical relays. This rapid response allows current to be interrupted before it becomes hazardous, which is crucial for effective circuit protection.
- **Wear and tear:** With no mechanical components, semiconductor switches can perform unlimited connect/disconnect cycles without degradation.

The transition from incandescent to LED lighting offers a useful analogy for the transition from electro-mechanical to semiconductor circuit breakers. The widespread adoption of LED bulbs that could be installed into existing sockets designed for incandescent bulbs allowed customers to gradually make the transition. In the early years when LED lighting had a high price premium, users could install LED bulbs only in high-use sockets where the efficiency gains justified the additional cost.

Similarly, development of SCBs that can be installed directly into electrical panels originally designed for electro-mechanical circuit breakers will allow a gradual methodical transition. However, this introduces significant challenges, the first of these being thermal management. Traditional circuit breakers based on mechanical relays have extremely low contact resistance, producing little heat during normal operation. Consequently, circuit breaker panels have minimal accommodations for the removal of heat, with limited air flow and no heat sinks. Given these constraints, SCBs designed for existing panels must generate minimal heat, necessitating a low effective on-resistance of the semiconductor switch.

The second challenge for SCBs is size. To be compatible with existing panels, SCBs must conform to the form factor of existing electro-mechanical circuit breakers, limiting the number of devices that can be installed in parallel to achieve the target resistance defined by the thermal constraints of the circuit breaker panel. These constraints drive the need for ultra-low $R_{DS(on)}$ devices in compact packages.

Qorvo's SiC JFET meets these stringent requirements with the lowest on-resistance by area ($R_{DS}\cdot A$) figure of merit of any device type in its voltage range, thanks to its simple structure.

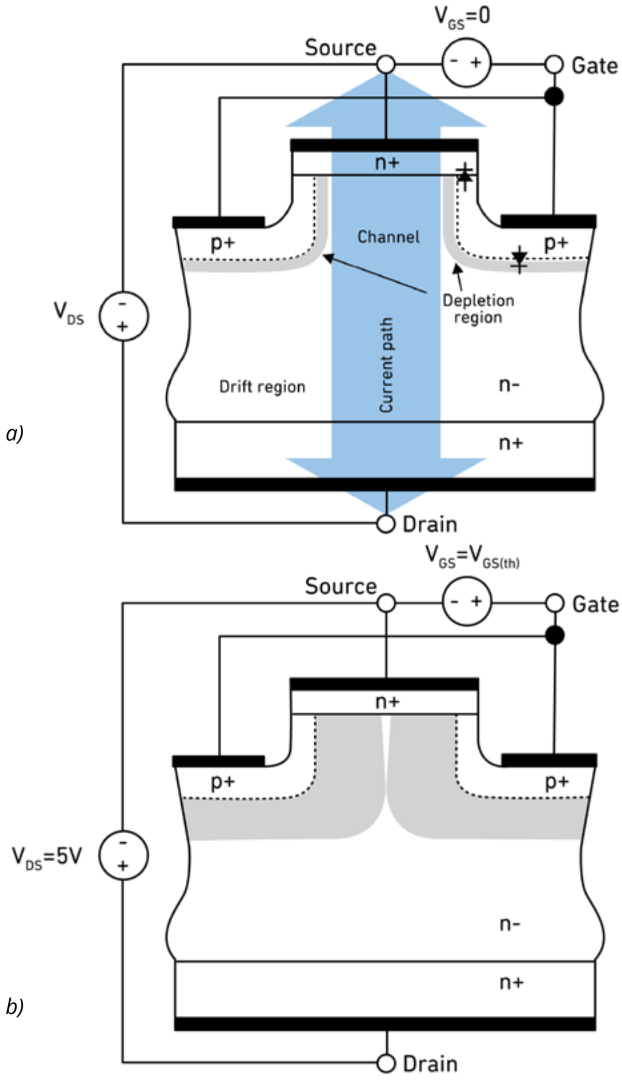


Figure 1: Vertical JFET cross section (a) without bias voltages, and (b) biases for $V_{G(th)}$ characterization.

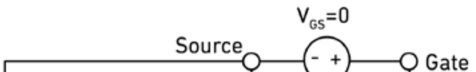


Figure 1(a) shows a simplified cross section of a Qorvo SiC JFET with gate-source voltage V_{GS} = 0 and drain-source voltage V_{DS} nearly zero. This represents one of thousands of parallel cells in a JFET chip with terminals labeled Source, Gate and Drain. The Qorvo SiC JFET has two PN junctions, thus two diodes: drain-to-gate and gate-to-source, shown in the figure superimposed across the corresponding PN junctions. In this unbiased state, a highly conductive channel exists between the Drain and Source, allowing electrons to freely flow in either direction, yielding the distinctive low on-resistance of the Qorvo SiC JFET.

Around each PN junction is a highly resistive depletion region, as mobile carriers have been repelled from the PN junction. The drain-gate depletion regions are indicated as gray areas in Figure 1. In (b), applying enough drain-source voltage motivates current to flow. However, current is almost zero, blocked by the expansion of the depletion regions due to the application of a negative gate-source voltage. When these depletion regions meet, the channel is pinched off.

The Qorvo SiC JFET is normally on (fully conductive) with no gate-source voltage applied and requires a negative V_{GS} to switch and remain off. While some semiconductor-relay applications benefit from this normally-on state, most require a default normally-off state. The normally-on Qorvo SiC JFET works well for both types, as the addition of a few simple components can keep it in a normally-off state, even without control power. But first, a couple graphs can help understand the construction of the Qorvo SiC JFET.

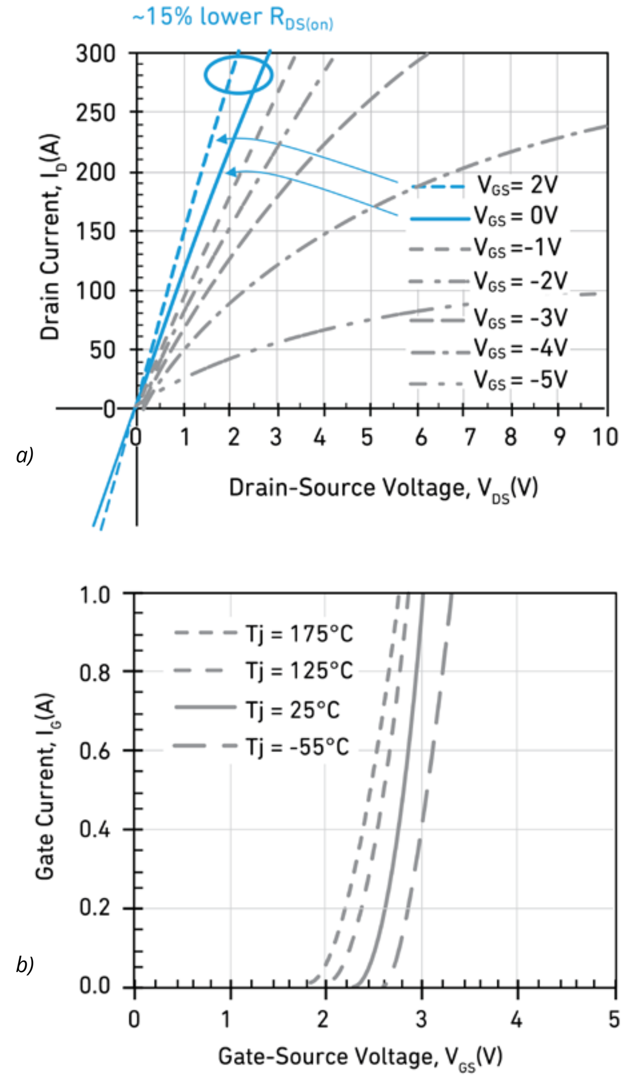


Figure 2: UJ4N075004L8S (a) output characteristics at 25°C, and (b) gate current versus V_{GS}.

Shown in Figure 2(a) are output characteristics with various gate-source voltages at room temperature of a 750 V, 4.3 mΩ SiC JFET in a TOLL (MO-229) package, part number UJ4N075004L8S. The typical part has a gate threshold voltage $V_{G(th)}$ = -6V.

With V_{GS} = -5V, the channel width is highly constricted by the depletion regions, so current flow is limited. Current increases slightly with V_{DS}, and the JFET is in “saturation.” At V_{GS} = -4V, the depletion regions are narrower, making the channel wider and thus increasing conductivity (reducing the on-resistance). This curve shows the effect of increasing V_{DS} and widening the depletion regions, bending the output characteristic curve, until there is little increase in current versus V_{DS}. On the other hand, increasing V_{GS} decreases the width of the depletion regions, which widens the channel and increases conductivity. The figure shows curves corresponding to certain V_{GS} values, all the way to +2V, which is the last V_{GS} test voltage.

Note that in these figures, $R_{DS(on)}$ is on-resistance characterized at either V_{GS} = 0V or V_{GS} = +2V. A slightly positive V_{GS}, such as 2 to 2.5 V, further shrinks the drain-gate depletion regions and reduces $R_{DS(on)}$ by 15%, depending on operating conditions. Commonly called overdriving, it’s an easy way to minimize JFET $R_{DS(on)}$ without risk of damage or parameter drift — yet another advantage of the Qorvo SiC JFET in applications that require cool operation and a long service life.

The on-resistance temperature coefficient (TC) is positive, which, combined with controllable switching speed via the gate drive, makes paralleling easy. However, the strong TC must be considered when selecting parts and deciding how many to parallel. Even at high operating temperatures, Qorvo’s SiC JFET has substantially lower conduction loss per package size compared to competing device technologies.

Figure 2(b) shows the gate current versus V_{GS} for Qorvo’s UJ4N075004L8S, where the SiC JFET gate-source diode is forward biased. The temperature-dependent diode “knee voltage” is clearly visible, and the slope corresponds to the JFET gate resistance, which is 0.4 Ω. V_{GS} is in a range of 2 to 2.6 V with IG in the milliamps range and temperature spanning from -55 to 175°C. This graph also shows the JFET’s gate-source diode forward voltage temperature coefficient of -3.2 mV/°C, which can be used to sense the JFET chip temperature with a simple differential amplifier circuit.

The simple structure of the Qorvo SiC JFET yields unrivaled conductivity, but this simplicity also delivers unmatched reliability and durability. Current flows directly through SiC material that is doped with highly mobile electrons. There is no PN junction in the current path, nor is there surface current. This design ensures no degradation mechanism, hysteresis or unusual dynamic effects. Additionally burn-in is not needed. As long as safe operating conditions are not grossly exceeded, the Qorvo SiC JFET’s operation remains consistent even after many years.

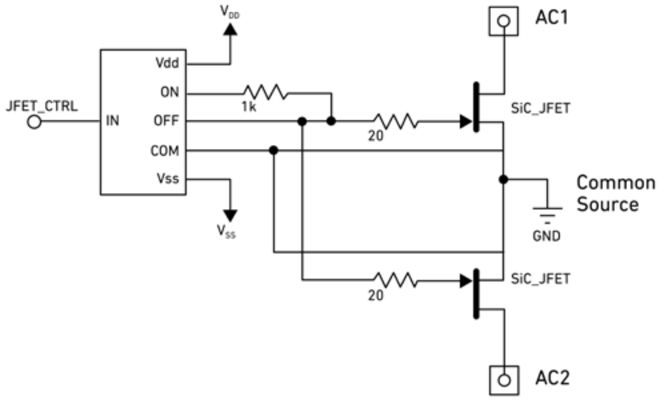


Figure 3: Direct drive circuit with bidirectional blocking and normally-on state.

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One final trait results from the simplicity of the Qorvo SiC JFET structure — robustness. The SiC material can withstand high internal temperatures, hundreds of degrees Celsius without parameter shift, provided the energy remains within safe limits. This enables the Qorvo SiC JFET to switch off very high currents, including short circuits, for any number of cycles. Electromechanical circuit breakers and relays endure a limited number of emergency-switching cycles, sometimes only one.

Figure 3 shows a bidirectional blocking configuration with simple overdrive of the JFETs. This circuit is normally on, meaning that the JFETs are on when there is no gate drive power. An off-the-shelf gate driver directly drives each JFET gate, with no need for voltage regulation. The value of the on-state resistor depends on the desired JFET gate current; at least 1 mA is enough to overdrive the JFET gate, while 5 mA or more is recommended for easy on-chip temperature sensing. Note that the switch-on speed is relatively slow with the large on-state gate resistance, but this is desirable for many SCB and relay applications.

The JFET gate driver's negative supply voltage can range from a minimum -30 V to a recommended maximum of -12 V for V_{SS}, or an absolute maximum of 2 V below the SiC JFET's minimum threshold voltage value specified in the datasheet. The positive supply voltage depends on the selected gate driver's undervoltage lockout (UVLO) rating. For example, a gate driver such as UCC5304 can have as little as 6 V for V_{DD}, allowing for adjustment of the on-state gate resistance accordingly.

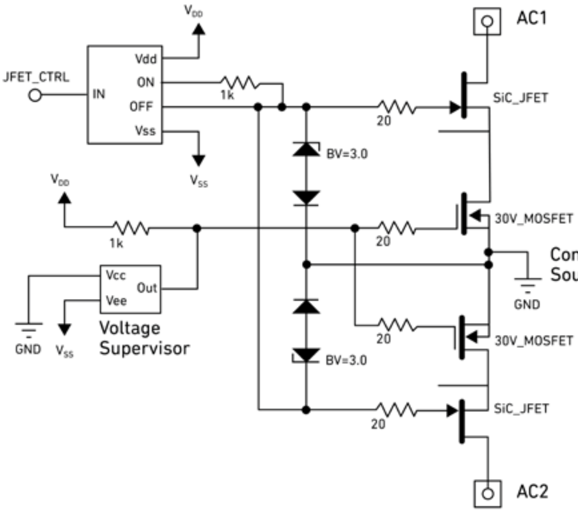

Figure 4: Direct drive circuit with bidirectional blocking and normally-off state.

Figure 4 shows a bidirectional blocking configuration, again with simple overdrive of the JFETs. A normally-off state is achieved by connecting a low-voltage silicon MOSFET in series with each JFET in a quasi-cascode configuration. An off-the-shelf gate driver directly drives each JFET's gate, while a voltage supervisor controls each MOSFET, ensuring they remain on when the gate drive supply voltage is within operating range. The voltage supervisor in the block diagram monitors the negative gate drive voltage, so the MOSFET remains off until the JFET can be reliably switched off by the JFET gate driver. Alternatively, the voltage supervisor could be substituted by a gate driver.

Similar to the circuit in Figure 3, the JFET's switch-on is through a large value gate resistor. The JFET gate-source diodes have a temperature-dependent forward voltage of 2 V to 2.5 V. Thus, the Zener diodes, with a breakdown voltage (BV) of 3V, will not activate, allowing 6 mA to flow into each JFET.

The diodes in anti-series with the Zener diodes allow the gate driver to pull the JFET gates negative. During normal operation, it is as if these diodes and the Zener diodes are effectively bypassed. Their main purpose is to switch off the JFETs in the absence of gate drive power, such as during startup. In this circumstance, as the voltage rises across the AC power terminals, the voltage rises across the normally-off MOSFETs. When the voltage exceeds the Zener BV plus the magnitude of the JFET threshold voltage, the JFETs are off, so no current flows, even if the voltage across the AC terminals reaches several hundred volts.

The JFET drive examples here are just a few of many possible implementations. Key points are:

- Simple gate drive, for both normally-on and -off configurations
- Design flexibility
- Use of readily available gate drivers and circuit components

A bonus feature of directly driving the JFET gate is on-chip temperature sensing using the JFET's gate-source diode. This T_J sense method uses the JFET chip itself, eliminating the need for a sense diode or other device either inside or outside the JFET package. This means that the temperature sensing is both highly accurate and responds quickly.

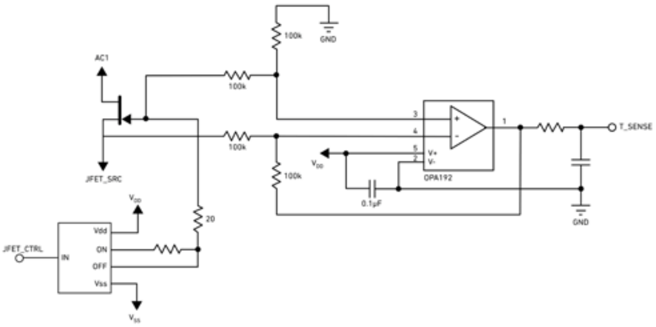

Figure 5: Temperature-sensing amplifier.

Figure 5 shows a differential amplifier that measures the JFET gate-source voltage V_{GS}. It includes a part of the gate drive circuitry from Figure 4, though some optional components are omitted for clarity, such as input-filtering capacitors and voltage clamp diodes. The amplifier in Figure 5 has unity gain, because V_{GS} varies within the range of many analog-to-digital converters (ADC) built into microcontrollers. To mitigate high frequency noise, a resistor-capacitor filter is used to smooth the amplifier output before transmitting the T_SENSE signal to an ADC input. The RC filter capacitor must be as close to the ADC input as possible.

This circuit can only sense the JFET chip temperature while the JFET is on and being overdriven. Note that regulating the current into the JFET gate, or the gate supply voltage, is unnecessary. For example, suppose the output of the gate driver is 15 V, and the on-state gate resistance is set so that 6 mA flows into the JFET gate. At that gate current, Qorvo's UJ4N075004L8S JFET has a VGS temperature coefficient of -3.2 mV/°C. The JFET VGS self-regulates based on chip temperature with a maximum range of 0.736 V for a temperature span of 230°C (-55 to 175°C). A usual temperature span would be about 100°C, corresponding to a range for V_{GS} of about 0.32 V, which is very small compared to the +15 V drive voltage. Therefore, the current into the JFET gate can be considered as constant with little error in the temperature measurement. This is a very simple, low-cost circuit that, along with overdriving, takes full advantage of the Qorvo's SiC JFET features.

In conclusion, consider a rhetorical question: Imagine that today there are no existing circuit protection products, and they must be developed from scratch. In this race to market, electromechanical breakers are in one lane, and semiconductor circuit breakers are in the other. Which one wins? Your answer to that question could shape the future of circuit protection.

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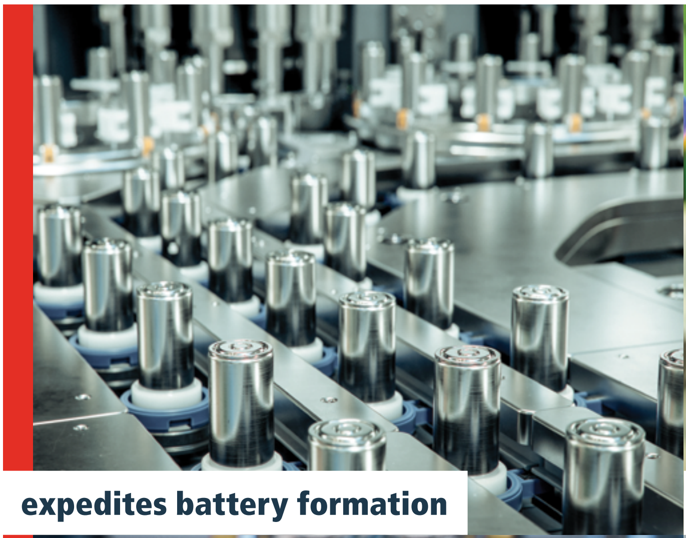

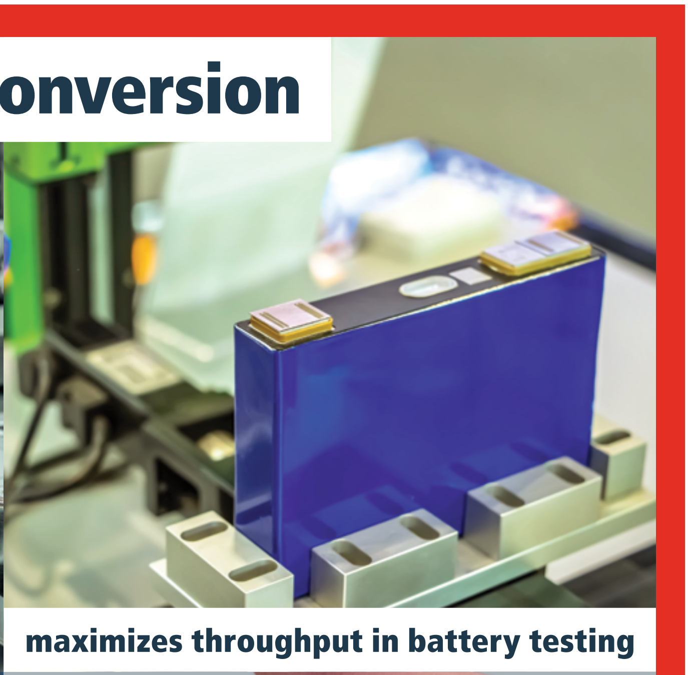


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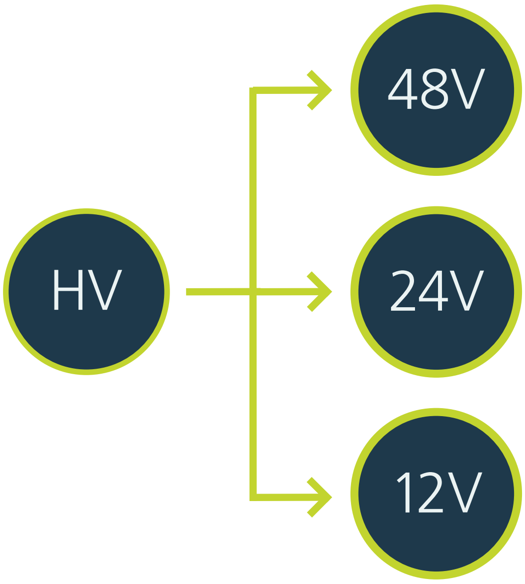
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The Impact of Direct Liquid Cooling on Building Power Semiconductors

The challenge in power electronics is to achieve higher power throughput in smaller at reduced cost. These often contradicting targets lead to compromises. Higher currents lead to higher thermal stress in a given device, reducing the lifetime.

By Dr.-Ing. Martin Schulz, Global Principal, Application Engineering, Littelfuse

To counteract, solutions with lower losses can be considered like replacing IGBTs by SiC-MOSFETs. However, the solution becomes more expensive. Another obvious method is improved cooling. However, insulating substrates put physical limits to the thermal transfer. The workaround? Drop the insulation requirement.

State-of-the-art

The most common semiconductor modules feature direct copper bonded substrates (DCB) with insulating ceramic layers. A setup like this can carry multiple dies as structuring the upper copper layer allows handling different potentials. Figure 1 schematically depicts such an approach. In contrast, high-power disc-devices are often combined with electrically active cold-plates as it is sketched in Figure 2.

The dominating thermal resistance within a setup as given in Figure 1 is provided by the ceramic layer. High-performance ceramics like aluminum nitride (AlN) feature thermal conductivities in the range of up to 180 W/(mK). Still, the thickness needed to achieve the necessary isolation results in a large thermal resistance. The setup in Figure 2 improves the thermal performance as no electrical insulation between the power semiconductor and the heat-sink is involved. As a consequence, an electrically non-conductive cooling liquid like de-ionised water/glycol mixture needs to be used and it's insulating quality must be monitored and maintained.

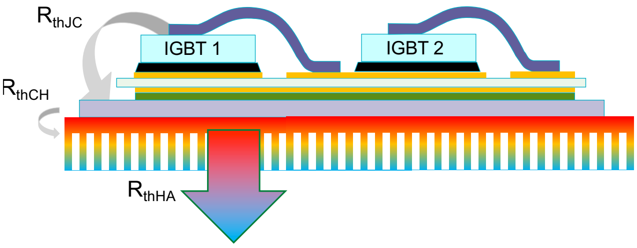

Figure 1: Structure of an insulated power semiconductor setup

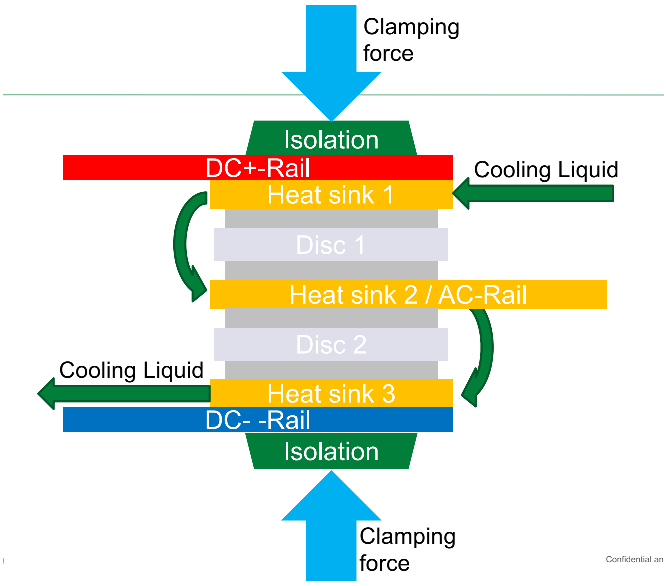

Figure 2: Power semiconductor arrangement with electrically active cold-plates

A different approach

To eliminate the dominating thermal resistance of the DCB, an approach was followed, soldering the IGBT-dies directly to a suitable liquid cold-plate of 40 x 80 mm². This way, the cold-plate becomes the electric connection to the IGBT's collectors. DCB substrates are used to mount the power-terminal at the emitter-side as well as the control-terminals. To overcome the limitations inflicted by the bond-wires, a test vehicle based on a different assembly-technology was built. In here, a different die with a solderable front-side-metallization was used. In turn, the bond-wires got replaced using interconnecting clips which are soldered to the IGBT's front side. As the clips cannot be soldered to the die directly, an interfacing pad is first soldered to the IGBT. The resulting test vehicle is pictured in Figure 3.

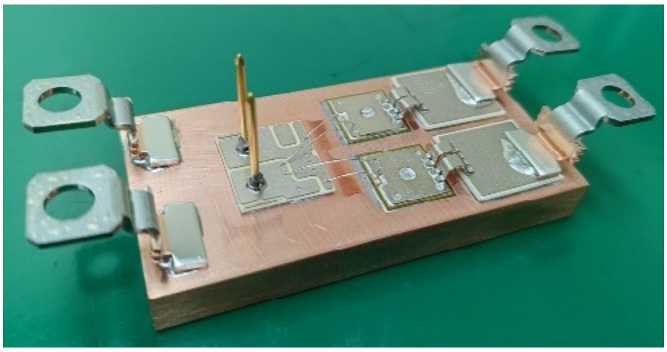

Figure 3: Clip-soldered test vehicle

An IR-Camera-based measurement was conducted, the result at 200 A per die can be seen in Figure 4.

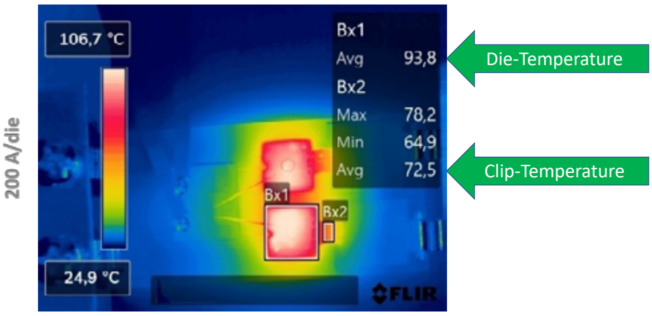

Figure 4: Thermographic measurement with clip-soldered material

It is obvious, that any limitations imposed by using bond-wires have been removed. The clip's temperature remains well below 100°C at current densities that are beyond the capabilities of bond wires the die could carry.

For the study, a standard die with a current rating of 150 A was used. Today's industrial boundary conditions include a maximum inlet temperature of 65°C and a maximum chip temperature of 175°C. From the measurements conducted, this leads to a maximum power loss density of 380 W/cm² that can be dissipated from the chip by the setup. It remains noteworthy, that the die, rated 150 A, was well within its thermal limits while handling 200A. For the targeted thermal conditions and 65°C inlet temperature, the maximum junction temperature of Tvj=175°C is reached at 250 A.

Electric testing
Though the focus of the study was on the thermal performance, the basic electrical behaviour of the setup was also tested, the result from a double-pulse-test is summarized in Figure 5.

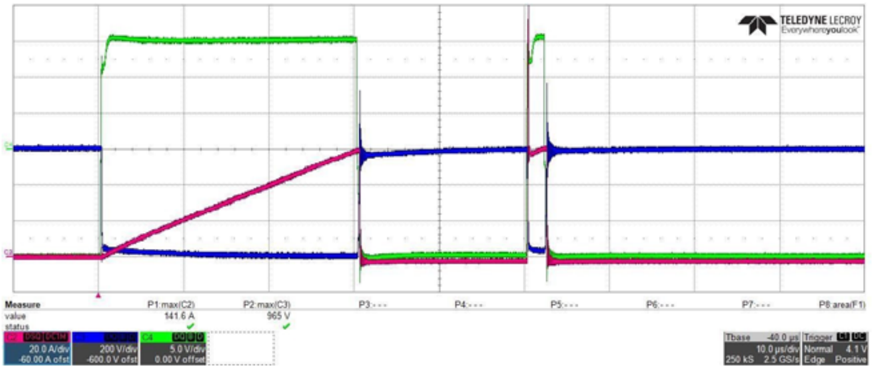

Figure 5: Results from the dynamic testing in double-pulse test equipment

The tests revealed a sufficiently clean switching but due to the nature of the test setup, no further details were investigated. Though the layout of the devices studied was not optimized for switching and a perfect switching behaviour was not expected, the results were still good enough to later be transferred into a potential series-development.

Cyclic load testing
The outstanding thermal performance is a key factor in increasing the lifetime of a power electronic component. From the second design, several devices were subjected to a power cycling test (PCsec) as defined in IEC 60749.

Figure 7: Results from the PCsec testing

The expectation was that the pad-and-clip assembly achieves a higher lifetime than a system using bond-wires as the failure mechanisms of bond-lift-off and bond-heel-crack are eliminated. However, as the pad is soldered to the chip's front-side, delamination of this interface is expected to happen eventually. The test was conducted with an inlet temperature of 12°C. In a cycle of 4 seconds with 50% duty-cycle, the chip temperature swing observed was 90 K with a load current of 250 A. Figure 6 reveals the outstanding thermal performance achieved and the low spreading of heat within the cold-plate.

The results from a long-tern test are depicted in the graph in Figure 7.

It remains to be noted, that the IGBT in this test had a rated chip current of only 150 A, so despite staying within the given thermal limits for chip temperature, the chip was operated well beyond parameters that would be used in a real-world application.

The end-of-life criteria for this test is an increase of the forward voltage of 5%. This value was reached after roughly 145.000 cycles. Classical solder-bond-technology reaches about 80.000 cycles under these conditions. As further potential for improvement is seen in the chip metallization as well as in solder alloys and solder processes, achieving at least twice the power-cycling capability compared to solder-bond devices does seem reasonable.

Potential applications and resulting benefits
From the structure chosen and power density achieved, it is obvious, that such a design is meant to operate in a high-power application. Especially applications that al-ready fea-

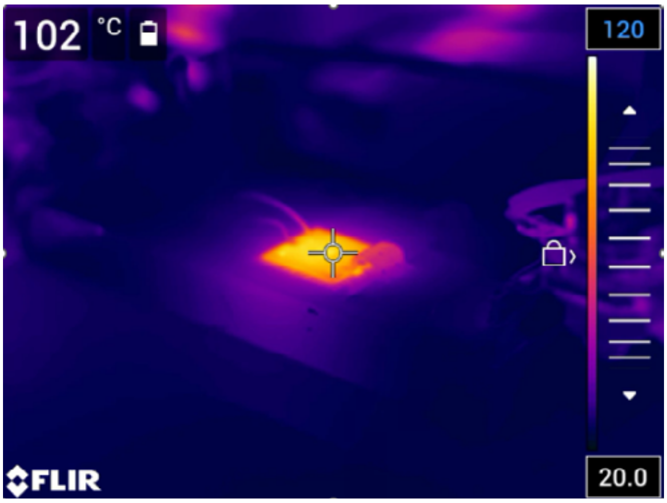

Figure 6: Thermal image of the chip during PCsec-Test

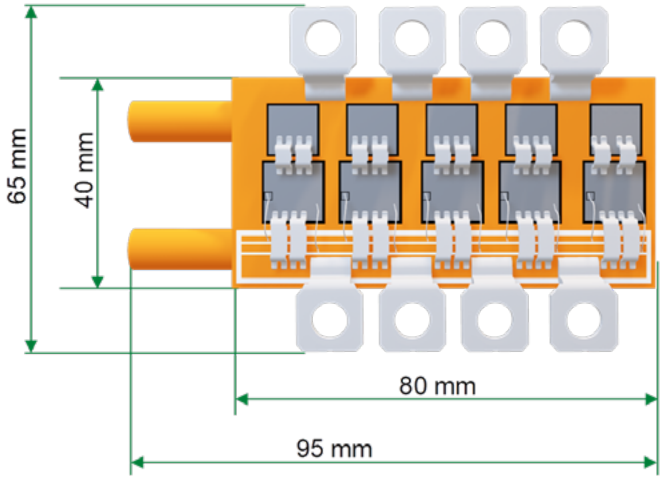

Figure 8: 1200 A-Device in non-isolated setup

ture liquid cooling and demand high power throughput can benefit from an insulated power semi-conductor arrangement.

Targets for such an approach can be found in renewable energy generation in windmills or in metal-welding by induction heating. With the heat sink forming the connection to the IGBT's collector, the scheme is a good choice for building single switches with high current carrying capabilities as schematically drawn in Figure 8.

Equipped with a 250 A-chipset, this version resembles a 1200 A single switch with an envelope of 123.5 cm³.

A half-bridge consisting of two such devices consumes about 250 cm³ of space. In comparison, high-power modules used today demand up to 700 cm³.

A further benefit arising from the integrated liquid cooling is, that the necessary surrounding housing is no longer burdened with the high temperatures commonly seen in power semiconductors. This opens a path to use lower-grade plastics, potentially even materials that are easy to recycle, which will be a major topic in the years ahead.

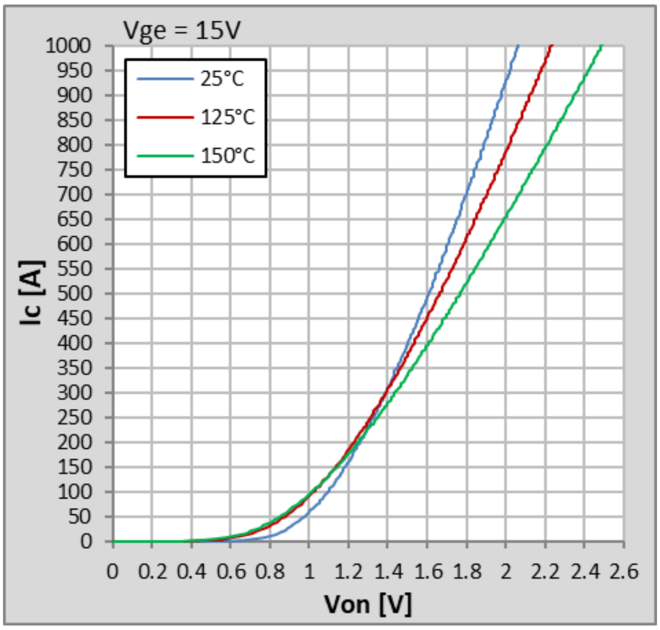

Figure 9: IC vs. VCE of a newly designed IGBT with high desaturation limits

As for the use of resources, a half-bridge built from the device in Figure 8 has a mass below 0.7 kg which is less than half the weight of a current design.

Sacrificing a fraction of the performance by replacing the copper heat sink using aluminum would allow for both, cost, and weight reduction.

Highly efficient cooling also is the key to fully exploit the capabilities of IGBTs with very high desaturation limits. The limiting triangle of forward voltage, switching performance and short-circuit-robustness spans the optimization area for IGBT-technology. Chips with low switching losses tend to have higher forward voltage and vice versa, as long as the short-circuit capability remains untouched.
The diagram given in Figure 9 reflects the forward voltage of an IGBT, optimized for extraordinary low forward voltage.

This 1200 V-chip is rated 200 A and in this point of operation generates 240 W of losses. Though the chip could withstand currents up to 450 A easily, the losses grow to 720 W or, in this case, 360 W/cm².

Such power loss densities in assemblies with ceramic isolation materials would lead to too high chip temperatures, even when high-performance ceramics were installed.

With the direct liquid cooling approach, up to 380 W/cm² have been achieved, making it possible to operate the chip in this point of operation without exceeding its thermal limits.

The device in Figure 8 thus would be able to carry more than 2 kA of current which would potentially reach the tolerable current density limits within the terminals used.

Conclusion
The omnipresent trend of increasing power density in power semiconductors as they are built today starts reaching physical limits due to the isolation requirement. To push these limits further, new methods to extract heat from power semiconductors more efficiently need to be identified. One way of doing so is direct liquid cooling combined with a suitable chip- and interconnection technology as presented. The shift from classical isolated assemblies to non-isolated counterparts opens the door to increase power density by a factor of 10, compared to today's options.

This is not limited to IGBT-technology but can be transferred to wide-band-gap semiconductors the very same way.

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Finding Irregular Effects in Control Loop Designs without Compromise

Stable operation in all circumstances is essential for power converters. Different working conditions, such as load steps, startup/shutdown sequences and input voltage variation, apply to most converter types. In addition to the standard feedback control loop, integrated pulse width modulation (PWM) controllers provide extended functions, such as line feed-forward loop control and soft-start control.

By Marcus Sonst, Senior Application Engineer focusing on Power Electronic applications within the Product Management for Oscilloscopes, Rohde & Schwarz.

Oscilloscopes with a sensible digital trigger and large memory such as the R&S MXO 5 from Rohde & Schwarz are perfect for analyzing the behavior of power converters

These extended control functions improve regulation for specific conditions. Such complex regulation systems require smart methods to ensure proper operation of the converter in all modes. For this task, extensive expertise and the right measurement tools are essential for identifying and locating unexpected events in the system.

A power converter's design and its stability need to be validated in all operational modes. Generally, PWM controllers provide multiple functions, which may increase complexity and therefore require a smart validation approach. Examples include line feed-forward loop control and soft-start control. Soft-start control is a specific mode: when the converter starts up, the positive duty cycle is gradually increased to ramp up the output voltage smoothly to limit inrush current and overall electrical stress.

During this timeframe, the duty cycle varies from very low numbers to a higher value until the output voltage has reached a steady state condition. Once the sequence is complete, the standard control feedback loop regulates the output voltage to the target value. In addition, a line feed-forward loop might be active to optimize the output voltage regulation while the input voltage changes rapidly. Both control mechanisms coexist, making it difficult to detect and locate unexpected or unstable operation. Noise naturally exists in switching converter designs and may lead to improper regulation of the loop. This instability in control loops can be detected by triggering on voltage variation or, better still, by monitoring the width of the positive duty cycle, since the duty cycle is used to regulate the power plant in order to keep the output voltage constant. A complex triggering capability is therefore mandatory to detect any irregular event in such a complex control system.

Oscilloscope with complex triggering capability is mandatory

For this challenging task, test engineers need an oscilloscope which is based on digital trigger technology. Rohde & Schwarz has equipped its R&S MXO 4 and the new R&S MXO 5 oscilloscope series with a sensitive digital trigger of 0.0001/div. They offer a resolution of up to 18-bit in high definition mode. Since two trigger conditions are essential to find variations of the positive duty cycle after the soft-start period has elapsed, the oscilloscope also allows the definition of complex trigger conditions. Figure 1 shows the trigger conditions at converter startup.

Trigger condition A is used to detect the end of the soft-start ramp and is configured as the window trigger, where the output voltage must be in a defined range. The type of the trigger for condition B can be based on PWM pulse width.

The width trigger will detect any values outside a defined range of the positive duty cycle. This can easily occur due to an improper design of the line feed-forward control filter. However, if the converter is in a steady state, there will be no significant duty cycle variations. If the positive duty cycle deviates from a valid range due to some unexpected event, condition B will trigger and the acquisition will be stopped. This helps to isolate this specific event and the user can discover the root cause of this irregular control event.

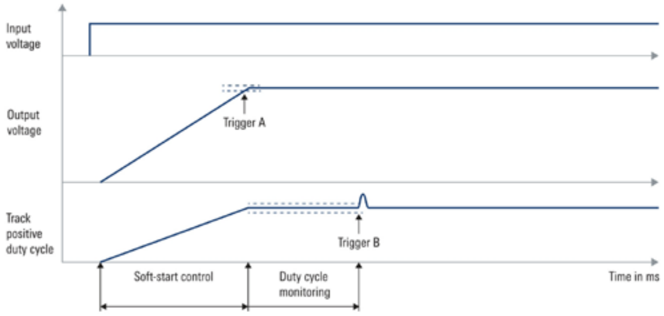

Figure 1: Complex trigger definition to detect irregular effects

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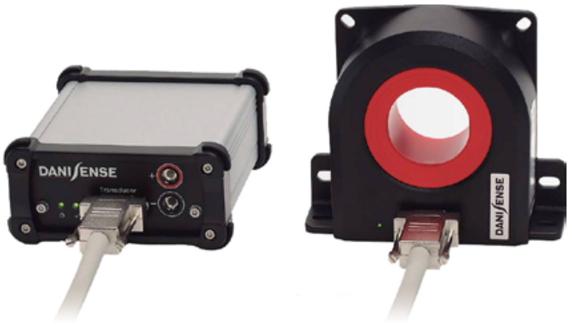


Complex triggering to analyze the behavior of a DC/DC switching converter

A DC/DC switching converter in full bridge topology with synchronous rectification is used to showcase the complex triggering with an R&S MXO 5. Handling with an R&S MXO 4 oscilloscope is identically. The isolated converter operates at a switching frequency of 100 kHz and converts the input voltage of 48 V to an output voltage of 12 V. The output current is specified to be a maximum of 8 A. The digital controller used in this application enables the user to activate, deactivate and modify the line feed-forward control.

Device setup step by step

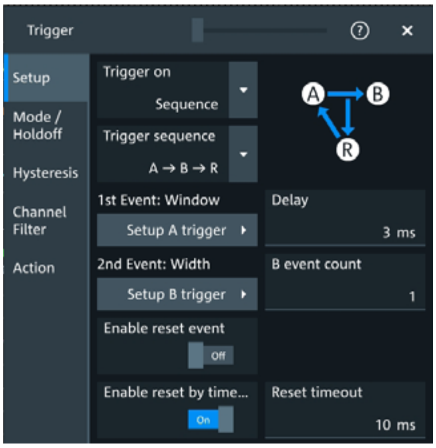
To configure a complex trigger:

- Set up a suitable channel, including proper probe selection
- Activate a trigger sequence and define an appropriate reset timeout (see Figure 2)
- Define trigger A as window type, including upper and lower level, to catch the end of the soft start during startup (see Figure 3)
- Activate the positive duty cycle measurement function and define the reference levels, e.g. 20/50/80 % of voltage
- Define trigger B as width type and set the width and delta time (see Figure 4)
- Activate the duty cycle measurement function, including the track function

Measurement of the load transient

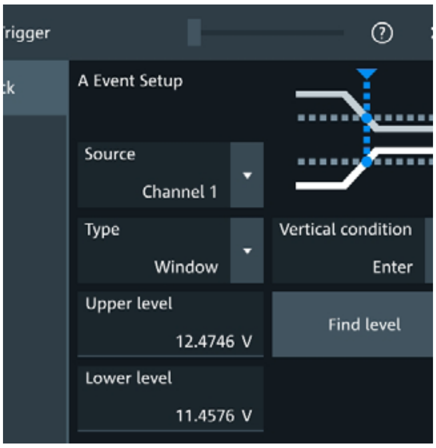
After being set up, the converter starts and the soft-start procedure is executed. As soon as the trigger detects a valid trigger for condition A, the instrument waits for any variation in the duty cycle measurement. Assuming a constant load after the soft start, the instrument will not trigger at condition B because the duty cycle should remain constant.

To showcase this complex trigger sequence, the line feed-forward function was activated inside the controller of the converter with an improper digital filter design. As a result, the instrument also triggered at condition B. The recorded measurement is shown in Figure 5, where the output voltage is measured on channel 1 and the input voltage is measured on channel 3. Channel 2 shows an internal signal of the controller, which reflects the input voltage to the secondary side. The M2 channel shows channel 2 filtered by a lowpass filter through math function. Furthermore, the PWM control signal (channel 4) and the track waveform of the positive duty cycle are displayed in the bottom window.



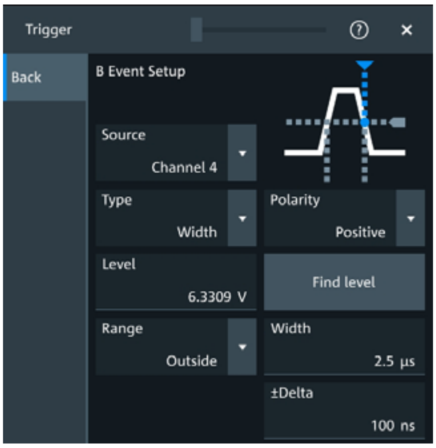
Trigger on: Sequence
Trigger sequence: A → B → R
1st Event: Window
Setup A trigger ▸
Delay: 3 ms
2nd Event: Width
Setup B trigger ▸
B event count: 1
Enable reset event: Off
Enable reset by time...: On
Reset timeout: 10 ms

Figure 2: Trigger sequence window



A Event Setup
Source: Channel 1
Type: Window
Vertical condition: Enter
Upper level: 12.4746 V
Find level
Lower level: 11.4576 V

Figure 3: Trigger event A window



B Event Setup
Source: Channel 4
Type: Width
Polarity: Positive
Level: 6.3309 V
Find level
Range: Outside
Width: 2.5 µs
±Delta: 100 ns

Figure 4: Trigger event B window

3 ms after the soft-start sequence has elapsed, the instrument triggers at condition B, because the duty cycle shows a positive step followed by a negative drop. This duty cycle variation is only present when the line feed forward is activated. The next step would be to optimize the acquisition length, which is now possible due to the complex trigger sequence. The result is shown in Figure 6.

In this case, more details become visible with increased accuracy, giving the user a better understanding of the system. Now, the user may start the process and can find the root cause very efficiently.

Summary

For identifying irregular events in the control loop of power converters, test engineers need an oscilloscope with digital trigger technology such as a R&S MXO 5 or a R&S MXO 4. These instruments enable them to define complex trigger events to isolate the root cause efficiently. In addition, they should choose an oscilloscope with large memory that allows them to add additional functions, such as the track on duty cycle, where a high sample rate is required over a long acquisition time. Here the R&S MXO 5 provides up to 1 Gpts per channel, allowing high resolution captures even at long record length. A R&S MXO 4 comes with a standard acquisition memory of 400 Mpts on all four channels.

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Figure 5: Startup of the converter and irregular control effects

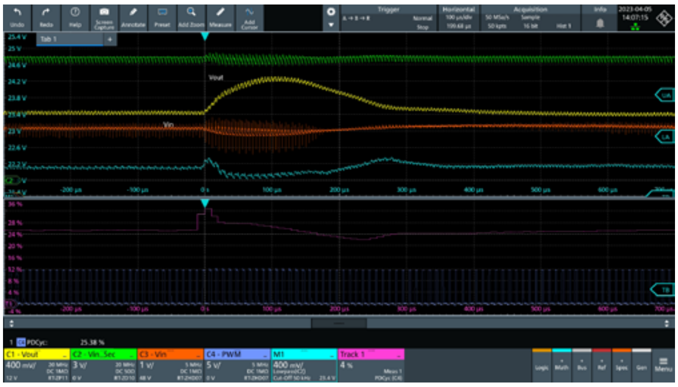


Figure 6: Irregular control effects at trigger condition B

qorvo

Accelerating Development of SiC-Based Power Converters, Such As EV Chargers

As the era of the internal combustion engine as the vehicle's primary power source fades, it is the electric motor that the automotive industry favours as the alternative. In turn, the automotive OEMs look to the semiconductor industry for the electronics innovations needed to deliver this electrified future. Battery electric vehicles (BEV) are currently the preferred approach, and everyone is looking to lead in the knowledge necessary to make them as appealing as possible. Although many get over-excited about the gadgets and features inside the car, vehicle range and charging remain the key concerns for consumers.

By Dr.-Ing. Matthias Ortmann, Chief Engineer, Toshiba Electronics Europe

Wide bandgap (WBG) technologies, such as Silicon Carbide (SiC), benefit from this change of power source in automotive and offer substantial advantages over traditional power devices, such as IGBTs, that we've previously relied on. The passive component manufacturers are working hard, too. Innovation in inductors helps to ensure the benefits of WBG as a faster switching topology to deliver more range and faster, more reliable charging technology.

All of this is backed by tangible demand. Revenue from electric vehicles (EV) is expected to reach over $620 billion in 2024 and grow at 10% per year[1], which will see more than 13 million BEVs added to our roads by the end of the decade. With new generations of SiC MOSFETs being released and improved passives regularly being rolled out, most engineers will be wondering how to effectively and efficiently evaluate the benefits they offer.

Commonalities in EV Power Converter Blocks

One area of focus is EV charging. Both BEVs and plug-in hybrids (PHEV) have an onboard charger (OBC) supporting currently power ranges of 3.6kW up to 22kW. These can be supplied with AC through a dedicated wall box or charging station at home, on the roadside or car park. For vehicles parked at home or work, it's an ideal method for topping up while the vehicle is at rest. When it comes to longer journeys, fast charging en route is provided by DC chargers. Delivering 40 – 300kW or even more, these bypass the OBC to deliver an 80% charge in around 20 to 60 minutes.

In both cases, the basic structure of the charger is the same. AC is fed into a power factor correction (PFC) unit followed by a DC/DC converter that supplies the vehicle battery's charging circuitry (Figure 1).

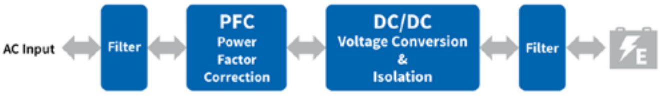


Figure 1: Basic blocks of an EV charging system.

Power efficiency is vital to minimise heat dissipation and save energy, while available space and design weight targets place pressure on power density requirements. Furthermore, EVs are seen as a potential power source to balance out electrical grid disturbances (vehicle to grid, V2G) or even provide power to homes in emergencies (vehicle to home, V2H). This means chargers need bidirectional topologies, leading us toward totem pole-style PFCs, and dual-active bridge (DAB) and LLC DC/DC converters. All these topologies make use of a bridge leg, and, looking at a motor inverter of an EV, this electronic element appears there, too.

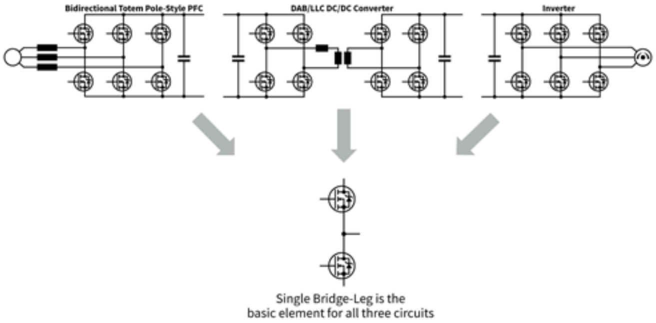


Figure 2: A bridge-leg is a common element of PFC, DC/DC, and inverter designs.

Modular Approach to Exploring SiC-based Designs

None of the topologies discussed are simple to design, with high voltages and currents at play during testing. However, the repeated circuit elements within these topologies offer a chance to use modularity as a means of rapidly evaluating different approaches. For example, the input inductors, single bridge legs, and the output capacitor can be isolated within the circuit of a PFC. Input and output voltage and current measurement, along with control of the SiC MOSFETs, can then be assigned to a fourth element performing system control. For this purpose, a microcontroller dedicated to digital power converter applications is ideal (Figure 3).

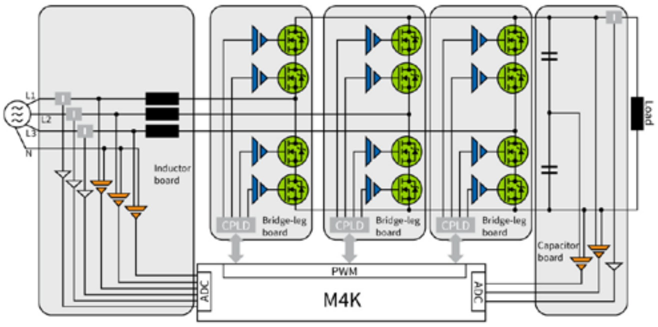
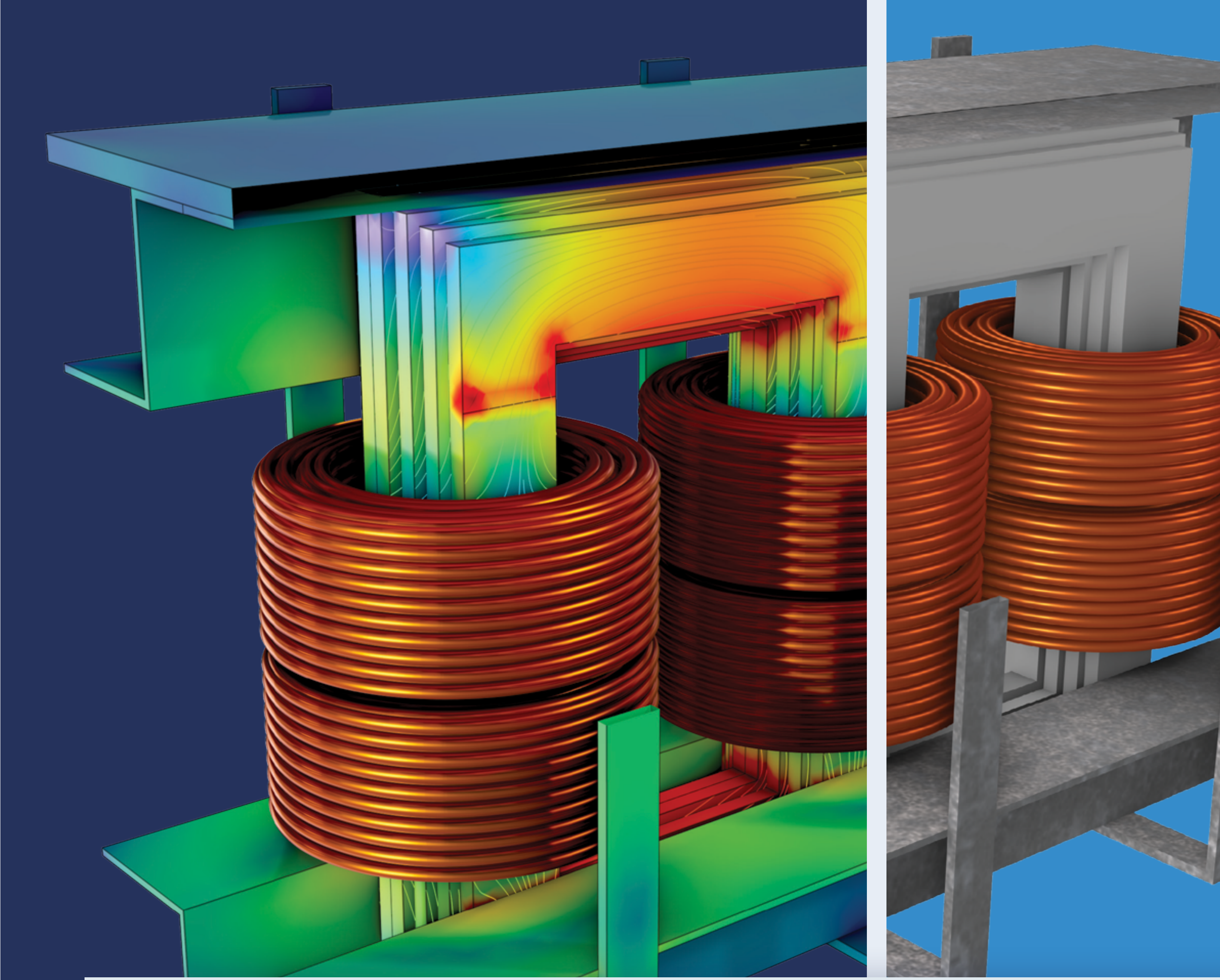


Figure 3: The PFC can be broken down into an input inductor, an output capacitor, bridge-leg, and a control block. Many blocks also find use in DC/DC converters and motor inverters.

This is the approach used to develop the feasibility study for the Modular EV Charger Reference Design Concept (Figure 4), that Toshiba has been undertaking to explore the development of a



compact design while meeting the power level requirements. It breaks the design down into seven printed circuit boards (PCB). At its core are the switching boards featuring four SiC MOSFETs in a three-level neutral point clamped (NPC) design. This supports sharing thermal load and voltage stresses across the switches and reduces volt-second ripple on the inductors. Two SiC Schottky barrier diodes (SBD), four gate drivers, and a complex programmable logic device (CPLD) to generate precise switching and the required four control signals round out the design.

The SiC MOSFETs include an on die integrated built-in Schottky Barrier Diode (SBD) with a forward voltage of just 1.35V. This integrated SBD is key to limit on-resistance changes over the operational lifetime. $R_{DS(ON)}$ × Q_{gd} (gate-drain charge) is also 80% lower than second-generation SiC devices, while the wider V_{GSS} rating of -10V to +25V simplifies gate driver circuit design.

Like in any power converter, optimal control of the switches over the application's lifetime is required. This is implemented using an optically isolated TLP5214 gate driver that delivers a ±4.0A output for fast switching, which is then paired with Toshiba's third-generation SiC MOSFETs. The driver also features an integrated active Miller clamp to avoid parasitic dV/dt-triggered turn-on.

Leveraging Features for a Compact Cube PFC Design

To achieve a compact cube design at the power levels demanded, interconnects are implemented in the high current paths using copper rails and the mechanical metal spacers that hold the boards together. This leads to an increase in the parasitic inductances of the implementation, limiting the switching speeds that can be used but keeps the PCB technology simple.

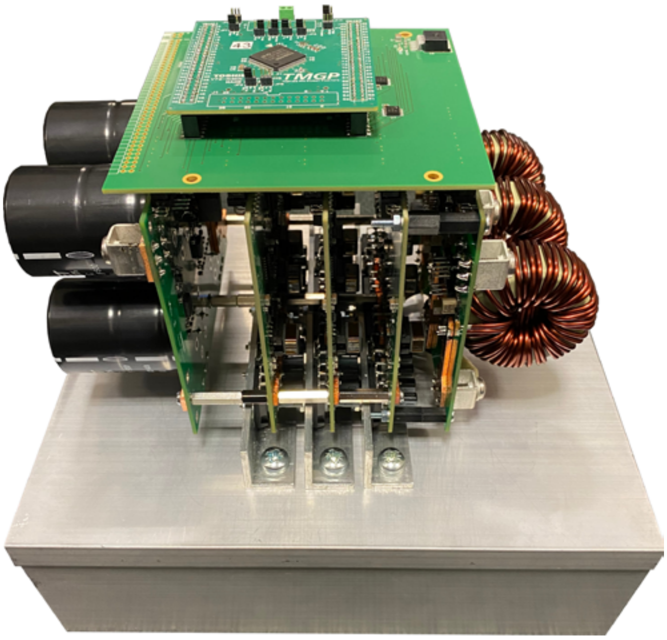


Figure 4: Details of the current-carrying mechanical interconnects and copper rails in the SiC Cube PFC design.

The inductor and capacitor boards (Figure 5) both feature the same current and voltage measurement circuitry. Current is measured using Hall sensors, while voltage is measured differentially using a TLP7820 isolated operational amplifier. On its input side, these use a sigma-delta analogue-to-digital (ADC) converter to drive an LED. The resultant optical signal feeds into an amplifier that is converted through a 1-bit digital-to-analogue converter (DAC) and low-pass filter. This approach offers high gain accuracy (±0.5%), small gain drift (0.00012V/°C), and low non-linearity (0.02% for V_{IN} = ±200mV). TLP7820 is UL/cUL recognized and VDE/CQC approved.

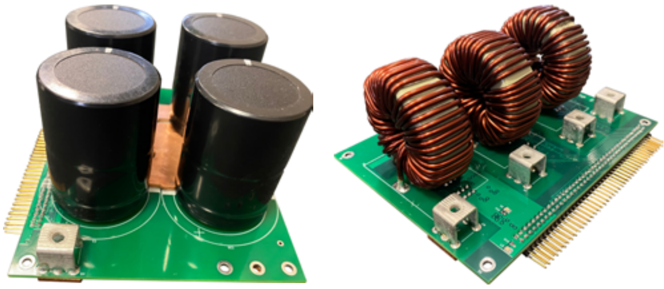


Figure 5: Both the capacitor and inductor boards feature the same current and voltage-measurement circuitry.

Traversing the bridge-leg, capacitor, and inductor boards is the controller board featuring a TXZ+ Arm® Cortex®-M4F microcontroller. What makes it particularly suited to digital power control is its advanced pulse-width modulation (PWM) modules that include a three-phase complementary output with dead-time control. Furthermore, it can be synchronized in hardware with analogue measurements made by the 12-bit on-chip ADCs. Three gain-selectable operational amplifiers are also available. The microcontroller also features a Vector Engine block that can offload and accelerate complex calculations like sin and cos but also Clarke and Park transformations, something beneficial as well for PFC and motor inverter applications.

High Power Density with Reusability

Leveraging the latest SiC MOSFET technology, this compact cuboid PFC design targets to deliver 22kW at a power factor of 0.99 and an efficiency of up to 99%. Measuring 140 × 140 × 210mm^3, that translates to a power density of 3kW/dm^3. Thanks to its modularity, the bridge-leg SiC MOSFET, capacitor, inductor, and microcontroller boards can easily be trialled in other power converter applications, thus easing the development burden. By creating this modular design concept Toshiba aims to support development teams new to WBG technology, and enable the exploration of the robustness, lower $R_{DS(ON)}$ over operational temperature, and higher switching frequency capabilities of SiC MOSFETs, which are still, for many, a new technology.

Next steps – further evaluation and development

Toshiba strives to offer comprehensive support to engineers and development teams venturing into the realm of SiC-based design. Typically, this support encompasses detailed documentation that covers every aspect of the reference design, including technical specifications, application notes, and design guidelines to facilitate a smoother development process.

The SiC Cube concept was initially presented at Bodo's Wide Bandgap event in Munich at the end of 2023. Presently, the SiC Cube feasibility study is assessing whether the modular and multi-level approach works effectively. At the moment, application support is available, with the schematics, board data and BOM information for SiC Cube having been established. It is expected that additional documents and resources will be available in the future.

References

[1] https://www.statista.com/outlook/mmo/electric-vehicles/worldwide

https://toshiba.semicon-storage.com

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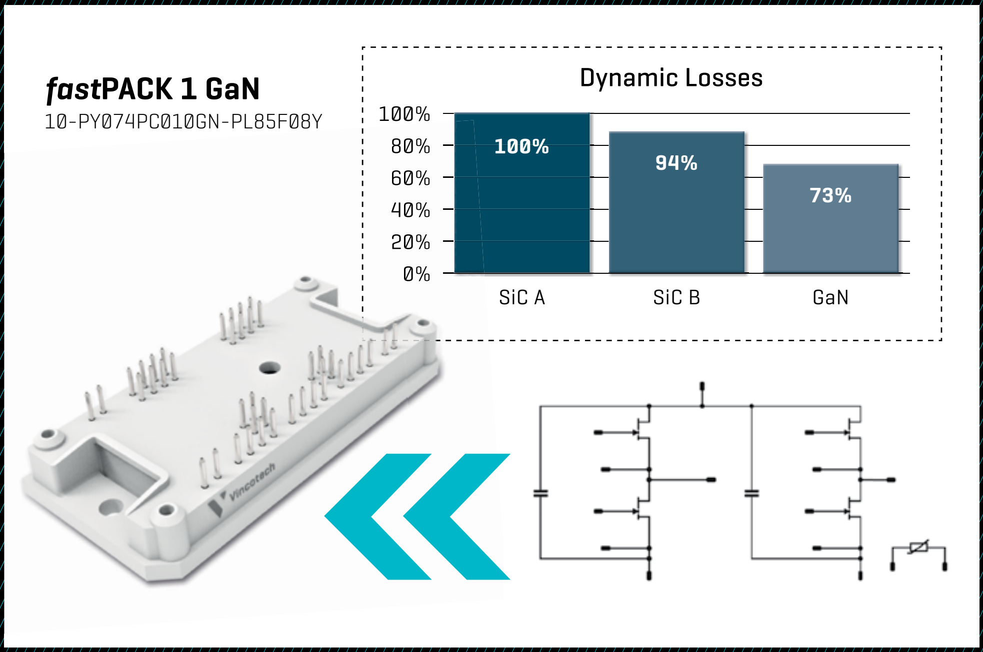
New *fast*PACK 1 GaN 2-in-1

Seeking for a highly efficient power conversion in isolated DC/DC converters, or DC/AC inverter stages, Vincotech´s new GaN-based power module is the answer. It offers a 2-in-1 solution, and can be utilized either as a 10mOhm H-Bridge or 5mOhm Half-bridge.

It is featuring E-mode GaN HEMTs chip tech for highest efficiency and power density and come in industry-standard package with low stray loop inductance. It works with external gate drives, giving a high design flexibility to engineers.

Main benefits

- Highest design flexibility with external gate driver, enabling slew rate control for low EMC
- Low voltage overshoots due to integrated snubber capacitors
- High power density and small footprint for soft switching above 500kHz
- Kelvin source pin and low inductive gate loop for clean switching behavior



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Unleashing the Power of AI to Transform PCB Design

AI-assisted PCB design offers a transformative approach that combines the power of automation, optimization, and decision support to streamline the design process, enhance design outcomes, and drive innovation in the field of electronic design.

By Steve Roberts, Innovation Manager, RECOM Power, and Tobias Pohl, co-founder and CEO of CELUS

One of the simplest ways to start artificial intelligence (AI) assisted PCB designing is to simply register on the CELUS Design Platform at: app.celus.io. The first step is that you are asked to complete a Project Summary which includes a description of your project, the selection of the functionalities it should contain, the intended application, which CAD Tool should the project be handed over to as well as the possibility to determine preferred and/or excluded parts and manufacturers. The Project Settings stage has two particularly important functions. Firstly, it causes the user to pause and take a step back to think about what they want to do before launching themselves blindly into the software. Secondly, it informs the platform about the essential parameters of the project so that it can tailor its advice and replies to better suit the project goals. The CELUS Design Platform was developed with artificial intelligence in mind from the very beginning, acting in many ways like a senior design engineer offering advice and knowledge to the next generation of design engineers, who may be bursting with ideas but simply lack the experience gained over many decades in the business.

It was this “companion” approach to project design and planning that attracted RECOM to be a partner with CELUS from the beginning. We could see the advantages of artificial intelligence when used as a time-saving tool –eliminating the drudgery of collating information, generating BoMs (bills of materials), creating netlists, and trawling through endless datasheets trying to find essential information such as efficiency figures, dimensions, or tolerances – work that could be safely assigned to a tireless AI assistant without giving the design engineer a feeling that they were no longer in control. However, in the intervening years, AI has moved onwards, and it now offers more than just assistance – namely collaboration.

For example, with the CELUS platform, once past the Project Settings and into the design stage, the software uses a familiar drag-and-drop style to create the system architecture block diagram. However, the lines linking the functional blocks could be power or data or both. It is not necessary to specify the connection type because the system understands how the functional blocks need to be interconnected. However, if the circuit designer has a particular preference, say, for an I2C data connection because they already have an existing interface firmware solution for that data type, then they can simply tell the system that that is what they want. The system will then choose the requisite interface when the schematic is generated. This integration of artificial intelligence in design platforms heralds a paradigm shift in PCB design because, unlike conventional PCB software, which merely flags design rule violations, AI-powered platforms offer a transformative approach. AI enables the system to leverage vast databases of information with ease, coupled with the intelligence to suggest informed solutions, effectively translating project goals into functional electronic designs. Therefore, RECOM is in the process of integrating our product portfolio, which includes around 30.000 parts into the CELUS knowledge database. By tapping into this wealth of data, the AI can make nuanced component selections tailored to the specific requirements of each project, thereby enhancing efficiency and optimizing performance.

Despite the undeniable potential of AI in PCB design, it’s natural for engineers to harbor concerns about its implications. Questions about job security and accountability often arise: Will AI take my job away? Will I be blamed if it makes a mistake? However, rather than being a threat, an AI assistant can serve as a dependable partner, capable of explaining its decisions and providing valuable insights. Its ability to justify choices fosters a collaborative environment where less-experienced engineers can learn and grow without feeling intimidated. Moreover, AI’s capacity for continual learning means that it evolves alongside its users, constantly improving and adapting to new challenges.

So, what can Artificial Intelligence in PCB design do, almost do, and not yet do?

Software platforms such as CELUS take the block diagram and find suitable solutions for circuit designers to evaluate and generate

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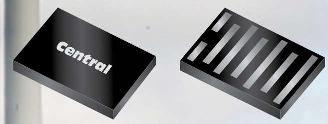
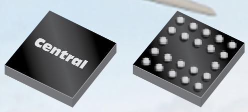


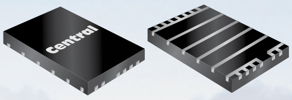
Top View Bottom View

CSP3.5X2 CASE



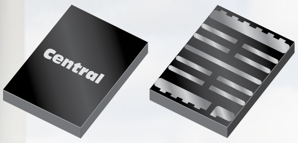
Top View Bottom View

CSP2X2 CASE



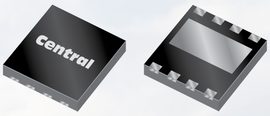
Top View Bottom View

CSP4X6 CASE



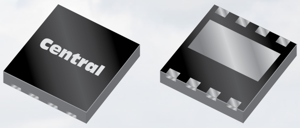
Top View Bottom View

CSP5X4 CASE



Top View Bottom View

DFN5X6A CASE



Top View Bottom View

DFN8X8 CASE

LOW VOLTAGE

		Maximum Ratings ($T_A = 25^\circ C$ unless otherwise noted)			Electrical Characteristics: ($T_A = 25^\circ C$ unless otherwise noted)						
	Central Item No.	V_{DS} (V) MAX	V_{GS} (V) MAX	I_D (A) MAX	I_{DM} (A) MAX	$r_{DS(ON)}$ (mΩ) MAX	$V_{GS(th)}$ (V) MAX	Q_g (nC) TYP	Q_{gd} (nC) TYP	Q_{gs} (nC) TYP	Package	Central Die Item No.
	CCSPG0420N*	40	6.0	20	100	4.0	2.4	15.8	8.6	1.9	CSP2X2	CPG005
	CCSPG0450N*	40	-4.0 to +6.0	50	200	1.5	2.3	28	4.6	6.2	CSP5X4	CPG006
	CCSPG1060N	100	-4.0 to +8.0	60	–	5.5	2.5	9.2	1.9	1.7	CSP3.5X2	CPG001
NEW	**CCSPG1560N***	150	-4.0 to +6.0	60	–	7.0	2.1	13	2.0	3.0	CSP4X6	CPG008
NEW	**CCSPG1510N***	150	-4.0 to +6.0	100	–	3.9	2.1	20	3.5	5.0	CSP4X6	CPG009

HIGH VOLTAGE

		Maximum Ratings ($T_A = 25^\circ C$ unless otherwise noted)			Electrical Characteristics: ($T_A = 25^\circ C$ unless otherwise noted)						
	Central Item No.	V_{DS} (V) MAX	V_{GS} (V) MAX	I_D (A) MAX	I_{DM} (A) MAX	$r_{DS(ON)}$ (mΩ) MAX	$V_{GS(th)}$ (V) MAX	Q_g (nC) TYP	Q_{gd} (nC) TYP	Q_{gs} (nC) TYP	Package	Central Die Item No.
	CDF56G6511N	650	-1.4 to +7.0	11.5	20.5	190	2.5	2.8	1.1	0.25	DFN5X6A	CPG003
	CDF56G6517N	650	-1.4 to +7.0	17	32	140	2.5	3.5	1.2	0.3	DFN5X6A	CPG004
	CDFG6511N*	650	-1.4 to +7.0	11.5	20.5	190	2.5	2.8	1.1	0.25	DFN8X8	CPG003
	CDFG6517N*	650	-1.4 to +7.0	17	32	140	2.5	3.5	1.2	0.3	DFN8X8	CPG004
NEW	**CDFG6558N***	650	-6.0 to +7.0	29	58	80	2.5	6.2	2.2	0.5	DFN8X8	CPG010
NEW	**CDF56G7032N***	700	-6.0 to +7.0	18	32	140	2.5	3.5	1.2	0.3	DFN5X6A	CPG011

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the schematic, BoM (bill of materials), floorplan proposal and footprints in a choice of different Electronic Design Automation (EDA) formats that are compatible with popular PCB Layout software such as Altium Designer, Autodesk Eagle, and KiCad. Once in the chosen native EDA format, the user can further modify the given solution to optimize the design, such as changing the component placement, adding polygons or copper pour to fill in the planes, setting component groups, changing the stack up, etc. These are the common design options that the layouter is familiar with and allows the user to take advantage of the head start given by the platform-generated prototype to make a fast time-to-market solution using their own custom design rules and preferences rather than having to use default settings. This handover process also optimizes the abilities of the different software platforms – AI is great to quickly turn an idea into a design, but the many specialized and advanced EDA platforms are ideal for generating the Gerber files containing the required CAM physical data such as the copper layers, solder masks, NC drill data, etc. Each to its own.

The boundary between the AI-assisted design and the layout software is not fixed. As the power of the machine learning algorithm increases, then more preparatory work can be done before handover. For example, when laying out a power electronics PCB, online calculators often need to be used to check the current capacity limits of tracks and vias. Existing EDA programs often have modules that can generate useful current density maps but can only make automatic changes to the layout if the voltage levels and component power demands are known. Thus, this part of the design process remains manual and relies heavily on the skill and experience of the designer to choose appropriate track widths and via aspect ratios. However, if this power consumption information could be made available to the artificial intelligence design assistant, this data could be synchronized with the layout software, so that machine-to-machine communication could be used to optimize the layout design automatically. Although such capabilities are not yet realized, ongoing advancements suggest they could become standard features soon.

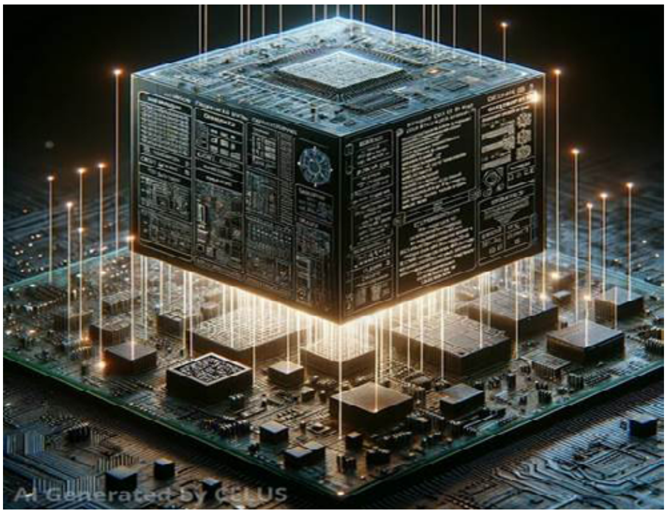

Figure 1: Concept of a CUBO™ Data module (AI-generated image)

Although a great deal of data can already be included in a cloud-based component database (for example, CELUS uses an enriched data block format that it calls CUBO™ to contain relevant information about a component application, such as signal mapping pin functionality, power supply requirements, etc. as well as any associated required components such as pull-up resistors, decoupling capacitors, crystals, etc. that are needed for full functionality), more data is often available in the individual component datasheet. Hence the current focus on AI-assisted data mining to extract relevant data from both text and graphical information held in the datasheets. However, this process is not easy. Different manufacturers place equivalent information on different pages of their datasheets, so a data miner would need to work its way through all the text and graphs and recognize that, say, an efficiency figure given on page 1 of Manufacturer A's datasheet is the same as the one given on the graph 2 on page 3 of Manufacturer B's datasheet. Sometimes the information is simply missing and often the information is comparable but not directly equivalent.

For example, Manufacturer A might give an isolation withstand voltage of 3kVDC for one second, while Manufacturer B might specify 1kVAC for one minute. Which one is better? The answer often depends on the application and project definition. The task is extracting useful and valid data from datasheets thus requires expert knowledge artificial intelligence algorithms, capable of handling inconsistent data. However, as AI algorithms improve, so does the ability to extract and interpret data accurately, paving the way for comprehensive datasheet data mining functionality in the coming years. This evolving landscape underscores the transformative potential of AI in PCB design, promising continued innovation and efficiency gains for the industry as a whole.

In conclusion, AI-assisted PCB design offers several significant advantages over traditional methods:

Speed and Efficiency: AI-powered design platforms streamline the design process by automating various tasks such as schematic generation, layout optimization, and component selection. This automation significantly reduces the time required to bring a product to market, enabling faster turnaround times and greater efficiency in design iterations.

Optimization and Performance: AI algorithms can analyze vast amounts of data to optimize designs for performance, reliability, and cost-effectiveness. By considering factors such as component specifications, signal integrity, and manufacturing constraints, AI-assisted designs can achieve higher levels of performance and reliability compared to manually crafted designs.

Enhanced Decision-Making: AI algorithms can assist engineers in making informed design decisions by providing real-time feedback and suggestions. This helps engineers identify potential issues early in the design process and explore alternative design options more efficiently, leading to better overall design outcomes.

Customization and Adaptability: AI-powered design platforms can adapt to the specific requirements of each project and user preferences. They can incorporate custom design rules, constraints, and preferences, allowing engineers to tailor designs to meet specific application needs while maintaining compatibility with industry standards and best practices.

Knowledge Transfer and Learning: AI-assisted design platforms can serve as valuable educational tools, especially for less-experienced engineers. By explaining design decisions, providing insights, and offering recommendations, AI systems can help engineers learn and improve their skills over time, contributing to professional development and knowledge transfer within organizations.

Risk Reduction: AI algorithms can help mitigate design risks by identifying potential issues, such as open or shorted connections and signal integrity problems before they become critical issues. This proactive approach to risk management can reduce costly design errors and rework, ultimately leading to more reliable and robust designs.

Overall, AI-assisted PCB design offers a transformative approach that combines the power of automation, optimization, and decision support to streamline the design process, enhance design outcomes, and drive innovation in the field of electronic design.

www.recom-power.com
www.celus.io

EPE'25

40 years of EPE conferences
1985 > 2025

Paris, France

March 31st > April 4th, 2025

The 26th European Conference on Power Electronics and Applications

cnrs GDR Groupement de recherche
SEEDS Systèmes d'énergie électrique dans leurs dimensions sociétales

The European Power Electronics and Drives Association is proud to announce that EPE'25 will take place in the La Villette Congress Center, part of the magnificent Cité des sciences et de l'industrie in Paris, France, from the 31st of March until the 4th of April 2025. In addition to the regular topics, EPE'25 will highlight six Focus Topics, with dedicated lectures and dialogue sessions, keynotes, exhibition, panel discussions, tutorials and technical visits.

Paper submissions in line with these Focus Topics are highly encouraged:

1. Electromobility – The powerful factor in reducing CO_2
2. Smart grids and renewable energy
3. Energy storage systems
4. Digitalisation, the powerful fusion of AI and IoT for sustainability
5. Sustainable and affordable power electronics
6. Energy transition and societal change

IMPORTANT DATES:
August 15, 2024: Provisional Paper Submission
November 15, 2024: Acceptance Notification
December 31, 2024: Full Paper Submission Deadline

Cité des sciences et de l'industrie | 30 Avenue Corentin Cariou, 75019 Paris

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Unleashing the Power of Diamond as a Semiconductor

Diamond has long been considered as the ultimate semiconductor for power electronics. In a global economy yearning for technology as a solution for climate change, power electronics is one of the enabling keys for the electrification, and therefore the decarbonation of our society. AI & data centers, mobility electrification, industrial electrification, renewable energy integration, energy storage, and green hydrogen production need suitable power electronics. Each application has its own constraints both technical, environmental, and economical.

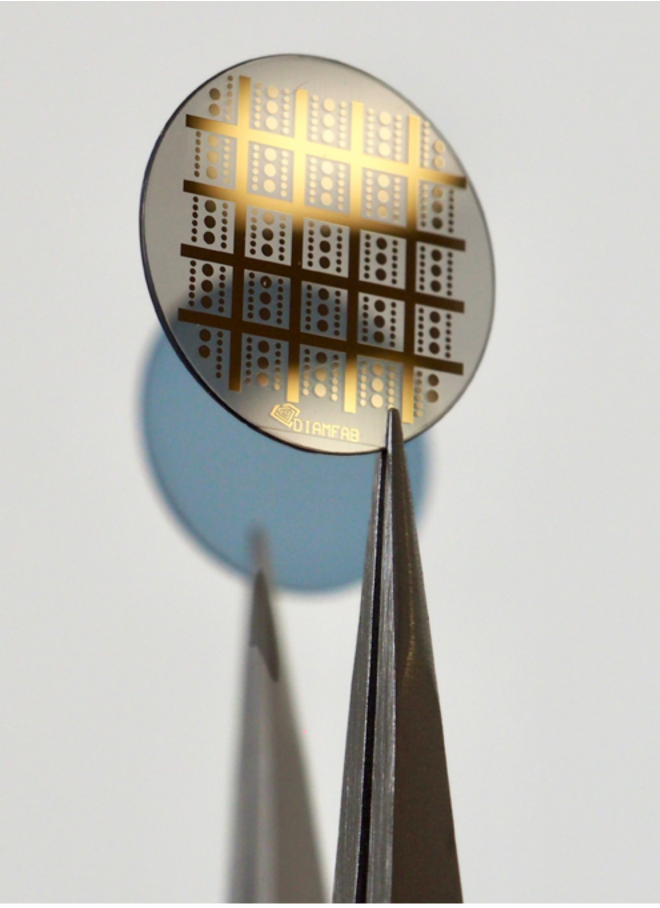
By Gauthier Chicot, CEO, and Ivan Llaurado, CRO & Director of Partnerships, DIAMFAB

So, what are the challenges in power electronics? We can argue that power electronics are a matter of tradeoff, not only at the component level, but at the system level. In an ideal world, every application would require power electronics without power losses, with a minimum size (volume and weight), and at low costs. The dilemma in power electronics is that customers cannot have it all, and it is physics fault.

Due to the physical properties of the semiconductor used in the components, there will always be losses during power conduction and switching, there will always be passive and cooling systems to extract the heat coming from losses and it comes at a cost. Therefore, there will always be a choice to be made to find a good tradeoff for every application.

For example, if priority is given to efficiency, this will have an impact on bigger sizes and lead to higher costs. Let's assume, the solution is to increase the voltage level of the system. As U = RI, and power losses are $P=RI^2$, if we double the voltage, we cut the current by a factor of 2, and losses are reduced by a factor of 4. However, by doing that, the components must adapt to the new voltage level. The RdSOn of the component follows (very approximately) the square curve with the voltage, so to keep the same resistance at doubled voltage, the surface required of the component will be increased also by a factor of 4. By doing that, the costs will be significantly higher than the previous components. But it is still not finished!

By increasing the surface, the switching losses will also be increased. A deep study to find the best tradeoff needs to be done. A deep study to find the best tradeoff needs to be done. Moreover, this example only assumes one possible solution, there are many others, but they come with their own drawbacks as well. Other factors can also impact the efficiency, such as junction temperature.



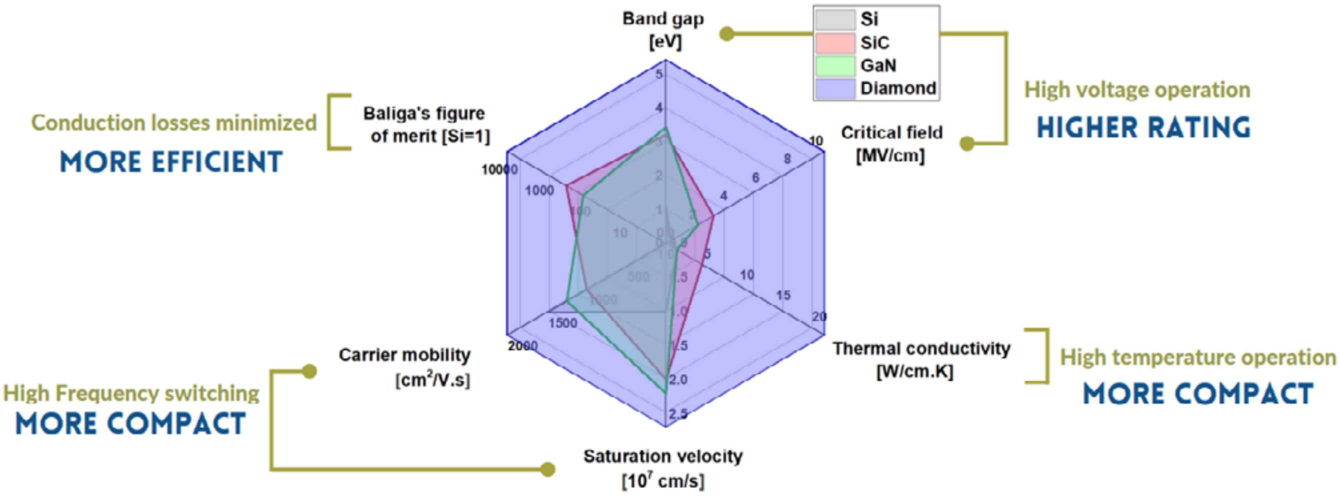


Figure 1: Please enter caption

XHP™ 2 CoolSiC™ MOSFET halfbridge module 3.3 kV

Infineon’s new high-power silicon carbide modules

Infineon is raising the bar in the field of power and technology with its two new 3.3 kV-rated silicon carbide (SiC) modules with robust .XT interconnection technology. These modules are designed to deliver high power (~1.5 MW) to applications with demanding mission profiles and challenging cycling requirements. The module FF2000UXTR33T2M1 offers a room temperature on-state resistance of 1.9 mΩ and nominal current rating of 1000 A and the FF2600UXTR33T2M1 offers a room temperature on-state resistance of 2.5 mΩ and nominal current rating of 750 A. Both are now ready for your order!

The 3.3 kV-rated CoolSiC™ MOSFET is optimized for fast switching with low oscillation tendency, which results in low total dynamic losses.

Key Features:

- CoolSiC™ MOSFET 3.3 kV
- Integrated body diode
- XHP™ 2 housing
- .XT interconnection technology

Benefits:

- Energy efficiency
- High power density
- Enhanced lifetime

Download the datasheets and find out more:

FF2000UXTR33T2M1

FF2600UXTR33T2M1

When turned on, the resistance of the component and the current going through generate joules losses. In most semiconductors, dissipating the heat and keeping the power semiconductor cooled (or as close to room temperature as possible) will prevent designers from overrating components and allow an overall higher efficiency. The cooling system required can be bulky, costly or both.

The same goes for size and volume reduction, or power density increase. The main drivers for reaching such goals are increasing switching frequencies (to reduce the size of passive components) and implementing active cooling systems, to reduce its size compared to a passive cooling system. The first action increases the energy losses, the second increases the costs. There is always a drawback.

Diamond semiconductor has the properties to make the tradeoff decisions much easier.

The main properties to be highlighted are ultra-wide band gap (5,5eV), exceptional carrier mobility (2000 & 1000 $cm^2 v^{-1} s^{-1}$ respectively for holes and electrons), breakdown voltage (10 MV/cm), best known heat conductivity (22 $W cm^{-1} K^{-1}$). These properties allow to increase voltage of the components, increase efficiency, reduce losses, and costs. It means that in order to reach a certain performance (let's say 1 mohm @1000V transistor), diamond will need much less surface area of material and less active thickness than current commonly used semiconductors.

To give an example with an image to better understand the ratio of performance between the different materials, imagine you have a diamond component of the surface equivalent of a basketball ball, with a given resistance for a 1000V breaking voltage capacity. The equivalent surface of silicon required to reach the same resistance for the same voltage rating would be a complete basketball field!

A very interesting characteristic of diamond is the resistance variation with temperature. Due to incomplete ionization at room temperature, the resistivity has a negative coefficient with temperature. It means that a diamond power transistor will have better performances at 200°C (or even at 300°C actually) than at room temperature. This characteristic opens up two questions. First, the parallelization of components needs to consider this characteristic. The risk being that as temperature rises on the component with lower resistance, the difference between the other parallel components increases and eventually all the current goes through to the same component, causing damage. Thanks to the exceptional thermal conductivity, the difference of temperature inside the die is less than 0,1 °C.

Second, and more important, is that the cooling system does not need to be as big as possible but just dimensioned enough to keep the junction temperature at the suited high temperature. This is a game changer because to improve the global efficiency, there is management needed to be done in heat extraction. To conclude, in terms of thermal management, diamond enables a system where efficiency peak is reached at high temperature and the junction temperature can be as high as packaging limitation. The cooling requirements are therefore drastically reduced.

Diamond semiconductor will also open up new possibilities for engineers when designing the system. Depending on the main target of the engineer (system cost vs efficiency vs volume), diamond components will be able to adjust to the needs. For example, if the main goal is to reduce costs, diamond components will allow to increase switching frequency compared to current, and therefore, decrease the passive components costs, also reducing the component costs.

Finally, diamond technology allows to decrease CO_2 emissions, not only during utilization, but also during the manufacturing steps. Compared to other semiconductor technologies that need very high temperatures (> 2000°C), diamond manufacturing requires electricity to create ideal plasma and pressure conditions for epitaxial growth. Unlike other semiconductor materials, there is no utilization of SF6 during the etching process, which is a major greenhouse gas. H2 and CH4 are the two main components required as raw materials, and both can be obtained with a very low level of carbon emissions: hydrogen can be produced from renewable energy (green hydrogen) and methane can also be obtained from biomass. We estimate that there is at least a factor of 10 in CO_2 reduction compared to silicon carbide.

At a glance, a system level diamond brings value on all key parameters for better power efficiency on three major elements:

- Thermal management simplification/reduction
- Better tradeoff between component & system competitiveness/ energy efficiency and volume and weight reduction
- Reduced CO_2 emissions for producing diamond wafer compared to other semiconducting materials

In terms of technology development, there are three historical roadblocks that need to be solved before expecting diamond to become a commercial reality: diamond wafer size, diamond wafer quality (in terms of dislocation and killer defects) and diamond doping.

These topics are being solved by the diamond industry. At Diamfab, we focus our development efforts on quality (default density reduction) and doping mastering. Growing a big-enough diamond crystal is not an easy task. However, while for other semiconductor technologies R&D investment has come from defense applications, the diamond industry is also leveraging knowledge from other industries, such as jewelry. The evolution is accelerating very quickly, 4 inch single crystal wafers (100 mm) have already been demonstrated, whereas a few years ago, only 3 mm wafers were available on the market.

In terms of the doping process, diamond is different from most other semiconductors. Diffusion or implantation processes are not suitable or recommended. The carbon lattice of diamond is so dense that dopant atoms such as boron, nitrogen or phosphorus do not penetrate by diffusion technique. On the contrary, dopant atoms damage the carbon lattice, making diamond non usable for power electronics. Therefore, diamond doping is done “in situ”, which means that the dopants are included while the carbon atoms are on the way to being organized as diamond. Today Diamfab masters the manufacturing doping process, from non-intentionally doped to the metallic transition (highly doped), with high homogeneity both in the x,y and z axis. Finally, crystal quality is also a topic that Diamfab is currently working on, and we hope to announce good news about this topic soon.

In a nutshell, the main technological bricks are solved or there is a clear view on how to solve them, both from the material and the component manufacturing side. We have also learned a lot from the developments performed in compound semiconductors.

In conclusion, at Diamfab, we are convinced that diamond as a semiconductor will be an alternative product this decade. We are confident that the promise of diamond is achievable. So far we have already achieved components with breakdown voltage above 1000V (on just 1.7 µm of diamond thickness) reaching current densities > 1000 A/cm^2; transistors with a breakdown voltage above 3,5 kV have been demonstrated too. Finally, we invite power electronics players, working with other semiconductors, from academia to integrators, to explore diamond potential and learn how they can apply their expertise to this technology that is about to come. There are many topics to develop with a promising future ahead.

www.diamfab.com

ECCE 2024
IEEE ENERGY CONVERSION CONGRESS & EXPO PHOENIX, ARIZONA, USA • OCT. 20-24

ECCE 2024

Phoenix, Arizona
October 20 – October 24, 2024

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Generating Negative Voltages – Why You Need Level Shifting in Buck-Boost Circuits

The magnitude of the negative voltage generated by inverting buck-boost circuits can be higher or lower than that of the available positive voltage. For example, –8 V or even –14 V can be generated from +12 V. When working with a switching regulator IC with an inverting buck-boost circuit, communications pins may be needed in the system design. If they are, it is essential for designers to remember adequate level shifting so that synchronization and enable signals can be utilized.

By Frederik Dostal, Field Applications Engineer, Analog Devices

Question:
Why is level shifting required?

Answer:
Inverting buck-boost circuits are commonly used for generating negative supply voltages from positive voltages. The most important step is ensuring that the negative voltages are generated correctly. However, additional level shifting circuits may be necessary if the power supply is controlled or supervised by the main application circuit. It has a reference to ground, while the GND pin of the inverting buck-boost power circuit is connected to the created negative voltage.

What to Consider When Designing Level Shift Circuits

The inverting buck-boost topology is one of the basic switching regulator topologies, requiring just one inductor, two capacitors, and two MOSFETs as switches. The switches can be driven with any buck regulator or controller. The availability of possible switching regulator building blocks is therefore large. Figure 1 shows the inverting topology with all the necessary components.

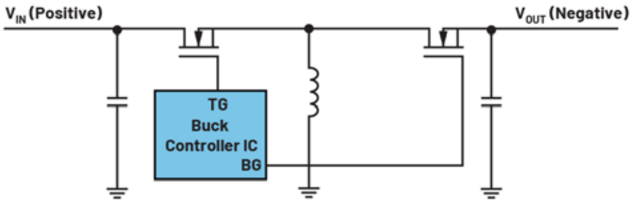


Figure 1: An inverting buck-boost topology for generating a negative voltage with a step-down (buck) switching regulator.

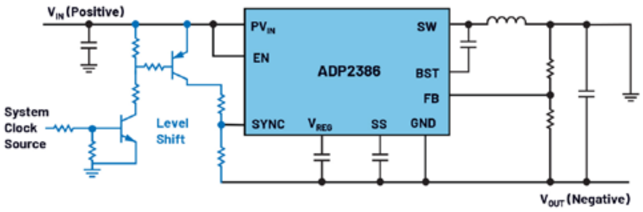


Figure 2: External level shifter for supplying the switching regulator IC with an external clock for synchronization.

Figure 2 shows a buck-boost circuit with an ADP2386 buck regulator. If a buck regulator IC is used for the inverting circuit, the ground connection of the IC is at the generated negative voltage. The original output voltage from the buck regulator is connected to the system ground. The buck regulator in the inverting topology references its own ground to the set negative voltage because the output voltage is connected to the system ground. The reference ground for the IC (GND in Figure 2) is not connected to the system ground. As a result, these two grounds are not at the same potential.

The switching regulator IC ground becomes the generated negative voltage. All pins on the switching regulator IC are now referenced to the generated negative voltage, rather than to the system ground. As a result, the communication lines and connections from the system to the IC and vice versa need level shifting to guarantee safe communication and prevent damage. Typically, the relevant signals are SYNC, PGOOD, TRACKING, MODE, EN, UVLO, and RESET. Figure 2 shows a possible level shift circuit with two bipolar transistors and seven resistors (in blue) for one signal. This circuit requires a certain amount of space and adds complexity to the circuitry as well as costs. Such a level shifter would have to be implemented separately for all signals previously mentioned. It is especially complicated when a switching regulator IC uses a digital bus such as the Power Management Bus (PMBus®). Then, the entire bus connection has to be operated with level shifting or galvanic isolation.

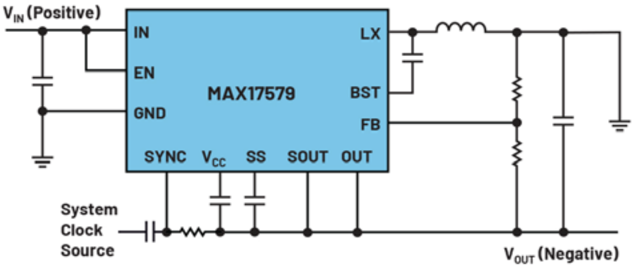


Figure 3: A MAX17579 designed as an inverting buck-boost regulator and with level shifting already integrated.

One way to avoid this external circuitry is to use a switching regulator IC that has been designed specifically for inverting voltages. Analog Devices offers a family of switching regulator ICs that are variations of buck regulator ICs. They are designed to facilitate communication between the system, that is, the entire electronic circuitry, and the inverting switching regulator IC. External level shifting as shown in Figure 2 is not needed.

Figure 3 shows the MAX17579 switching regulator IC, which generates a negative voltage from a positive voltage. As can be seen in Figure 3, the circuit is much more compact than the one in Figure 2.

Simulation tools such as LTspice® or the EE-SIM® design and evaluation environment can provide a better understanding of the regulation behavior and the potential differences in an inverting topology. Level shift circuits can be designed and optimized with these tools. ICs like the MAX17579 can also easily be simulated with the EE-SIM design tool.

www.analog.com

Line of Radiation Tolerant Analog Components

Apex Microtechnology is announces the launch of its radiation tolerant (RT) product portfolio. After extensive market evaluation and radiation test campaigns, Apex brings a range of military-grade RT devices to serve the space market and applications in radiation environments. The Apex rad tolerant portfolio will initially feature two operational amplifiers, PA07R and PA08R. Engineers designing with analog components for space applications will find these devices to be in-line with SWaP requirements, as well as feature little to no lead times.

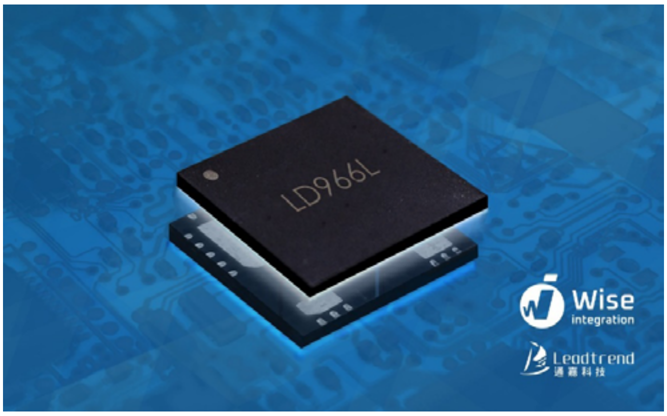
The PA08R is a high voltage power operational amplifier designed for output voltage swings up to ±145V with a dual supply, or a 290V single supply. This power amplifier delivers high accuracy via a cascode input circuit configuration. All internal biasing is referenced to a zener diode fed by a FET constant current source. Target applications for this POA include electrostatic transducers, deflection circuits and programmable power supplies. The PA08R is a hybrid product design housed in an electrically isolated, hermetically sealed 8-pin TO-3 metal package. For continuous operation under load, a heatsink of proper rating is recommended.

The PA07 is a high voltage, high output current operational amplifier designed to drive resistive, inductive, and capacitive loads. For optimum linearity, especially at low levels, the output stage is biased for class A/B operation using a thermistor compensated base-emitter voltage multiplier circuit. A thermal shutoff circuit protects against overheating and minimizes heatsink requirements for abnormal operating conditions. The safe operating area (SOA) can be observed for all operating conditions by selection of user programmable current limiting resistors. The amplifier is internally compensated for all gain settings. For continuous operation under load, a heatsink of proper rating is recommended.

www.apexanalog.com

GaN System-in-Package Targeting Rapid Consumer Device Charging

Wise-integration and Leadtrend Technology Corporation announced the release of a GaN system-in-package (SiP) supporting consumer electronics applications. Their collaboration's targeted application is a 65-watt USB PD adapter for high-speed charging of smartphones, laptops and other devices. The LD966LGQALVE High Voltage Multi-Mode PWM Controller of Flyback with GaN integrated includes Leadtrend's silicon die flyback controller and Wise-integration's 650V e-mode gallium-nitride (GaN) transistor die in a SiP. The SiP has passed 1,000 hours of operating life tests (OLT). The LD966L is green-mode PWMIC built-in with brown-in/out functions of a QFN8X8 package. It minimizes the component count, circuit space, and reduces overall material cost for the power applications. It features HV start, green-mode power-saving operation, soft-start functions to minimize power loss and enhance system performance. The LD966LGQALVE Evaluation Board features an overall peak efficiency of 93.02% and a power density of 22.7 W/in^3.



https://wise-integration.com

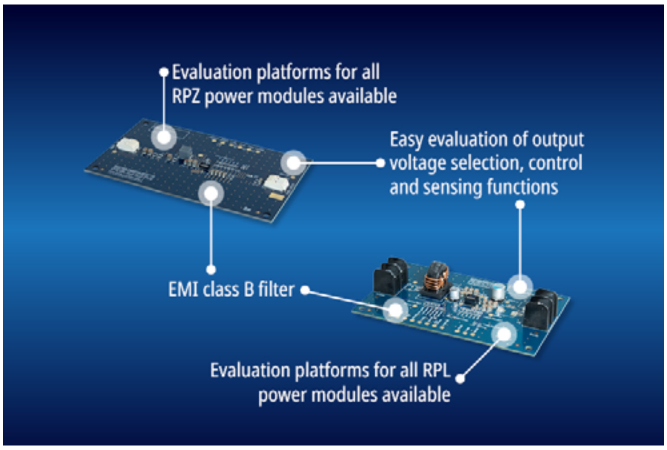
SiC Power Modules with a wide Range of Topology Options

WeEn Semiconductors has unveiled families of silicon carbide (SiC) MOSFETs and Schottky Barrier Diodes (SBDs) in TSPAK packaging. The TSPAK MOSFET and SBD devices address the demand for high-performance, compact and reliable power management in applications ranging from automotive charging and on-board charger applications to photovoltaic (PV) inverters and high-power-density power supplies (PSUs). Offering a variety of configuration options for maximum design flexibility, the SiC modules are ideal for applications such as EV charging, energy storage systems, PV inverters, motor drives, industrial PSUs and test instrumentation. Originally developed for automotive applications, TSPAK devices combine innovative top-side cooling capability with low thermal impedance to deliver enhanced thermal performance. By removing the PCB thermal resistance from the thermal dissipating path, the Junction-Ambient thermal resistance improves by 16-19%. This supports high reliability by enabling a greater number of power cycles than conventional packaging as well as providing the increased power densities demanded by compact system designs. Low circuit inductance and low EMC noise help to improve performance and reduce filtering requirements. The WeEn Semiconductors family of TSPAK MOSFETs features 650V, 750V, and 1200V options with resistances ranging from 12mΩ to 150mΩ. TSPAK SBDs are available with current ratings of 10 to 40A in 650V, 750V, and 1200V variants.

www.ween-semi.com

Evaluation Modules with Integrated Buck Converters

Evaluation of Recom's range of integrated buck regulators is now made easier with the new EVMs. Suiting models in the Recom RPL, RPH, and RPZ range with current ratings from 0.5 A to 20 A, the evaluation modules provide a way to characterize the converter performance in a realistic environment, both thermally and electrically. Filters are included to demonstrate compliance with EMI 'Class B' levels and all functions available in each converter can be exercised, e. g. output voltage selection and trim, remote sensing, on/off control, switching frequency selection, soft start, input under-voltage lock-out, and Power Good signaling. As the EVMs are designed to provide typical application heatsinking, the buck converters can be operated and evaluated at full load, and behavior is investigated under overload and overtemperature conditions. Alternate component positions are also included to allow experimentation to tailor EMC performance to the application and budget. The RPL, RPH, and RPZ products are a range of cost-effective integrated buck converters in QFN and LGA packages featuring advanced thermal and electrical design. The modules all have integrated inductors and feature a miniature footprint and profile down to 1.6 mm.



www.recom-power.com

1200 V SiC MOSFETs in SMD Packaging

Nexperia announced that it is now offering its 1200 V silicon carbide (SiC) MOSFETs in D2PAK-7 surface mount device (SMD) packaging, with a choice of 30, 40, 60, and 80 mΩ RDSon values. This announcement follows on from Nexperia's late-2023 release of two discrete SiC MOSFETs in 3 and 4-pin TO-247 packaging and is the latest offering in a series which will see its SiC MOSFET portfolio swiftly expand to include devices with RDSon values of 17, 30, 40, 60 and 80 mΩ in flexible package options.

With the release of the NSF0xx120D7A0, Nexperia is addressing the growing market demand for high performance SiC switches in SMD packages like D2PAK-7, which is becoming increasingly popular in various industrial applications including electric vehicle (EV) charging (charge pile, offboard charging), uninterruptible power supplies (UPS) and inverters for solar and energy storage systems (ESS). It is also further testimony to Nexperia's successful strategic partnership with Mitsubishi Electric Corporation (MELCO), which has seen the two companies join forces to push the energy efficiency and electrical performance of SiC wide bandgap semiconductors to the next level, while additionally future-proofing production capacity for this technology in response to ever growing market demand.

www.nexperia.com

Coreless High Current Sensors

Capable of measuring high DC currents from 2 kA up to 42 kA without surge current limitations, the Open Loop Coreless Integral (OLCI) sensors from LEM feature a large aperture for accurate measuring of high currents on large busbars, with up to 1 MHz bandwidth for high frequency applications. They are also significantly lighter (80%) and more cost effective than open loop or closed loop current transducers operating within the same current measuring range. Two versions of the OLCI high current sensors are available from LEM – the FRS model supporting primary busbar apertures of 104 mm x 22 mm and the FL for apertures up to 300 mm x 100 mm. Because it is a split transducer, the FL can be opened and attached directly anywhere on the busbar without the need to open the busbar, making it easy to install and maintain. With no magnetic core, no secondary copper winding, an integrated Rogowski coil and an array of Hall elements, the FRS sensor slashes raw material costs and reduces power losses. Equally suited to trackside and onboard traction applications in the railway industry as they are for high power wind turbines and hydrogen electrolysers, the sensors can also be used on industrial low-voltage and medium-voltage variable frequency drives, in induction welding applications, and for DC grid monitoring.

www.lem.com

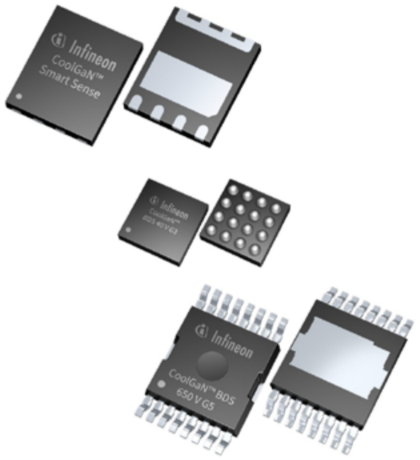
Rugged 500 W AC/DC Power Supplies utilizing Conduction Cooling for harsh Environments

P-DUKE has launched its XTBF500 AC/DC power supply series, available in open frame or enclosed form. The XTBF500 integrates the TBF500 full brick 500 W AC/DC power supply and its peripheral circuits, such as EMC filters, start-up current limiters, large capacity capacitors, and aluminum substrates, to achieve the concept of "easy to use." The XTBF500 series features a universal input voltage range of 85-264 VAC. The output voltage is 12, 15, 24, 28, 48, and 54 VDC, adjustable within a range of +10%/-10% via potentiometer. It also features slope current sharing to provide over 500 W of power by paralleling multiple modules, as well as complete protection functions, including overcurrent protection (hiccup mode), short circuit protection (auto-recovery), and output overvoltage protection (latch). XTBF500 has integrated all peripheral devices together to combine the advantages of a full brick module and a complete AC/DC power supply, in compliance with EMC standard EN/IEC 50032 Class B (CE Class B, RE Class A), start-up inrush current limiter function, and OVC III (overvoltage category). By conducting cooling on the system chassis, it can operate at full load up to 40 degrees to cope with harsh applications and demanding environments. The XTBF500 is designed for challenging operating conditions and is suited for various applications such as 5G communication, ESS, defense, robotics, and factory automation.

www.pduke.com

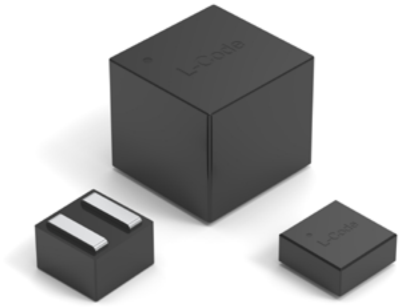
Bidirectional Switch and Smart Sense

Infineon Technologies announced two CoolGaN™ product technologies, CoolGaN bidirectional switch (BDS) and CoolGaN Smart Sense. CoolGaN BDS is said to provide "exceptional soft- and hard-switching behavior", with bidirectional switches available at 40 V, 650 V and 850 V. Target applications of this family include mobile device USB ports, battery management systems, inverters, and rectifiers. The CoolGaN Smart Sense products feature lossless current sensing, simplifying design and further reducing power losses, as well as transistor switch functions integrated into one package. They are ideal for usage in consumer USB-C chargers and adapters. The CoolGaN BDS high voltage feature a true normally-off monolithic bi-directional switch with four modes of operation. Based on the gate injection transistor (GIT) technology, the devices have two separate gates with substrate terminal and independent isolated control. The devices are suited for back-to-back switches in single-phase H4 PFC and HERIC inverters and three-phase Vienna rectifiers as well as for single-stage AC power conversion in AC/DC or DC/AC topologies. The CoolGaN BDS 40 V is a normally-off, monolithic bi-directional switch based on Infineon's in-house Schottky Gate GaN technology. It can block voltages in both directions, and through a single-gate and common-source design, it is optimized to replace back-to-back MOSFETs used as disconnect switches in battery-powered consumer products.



www.infineon.com

Expanded Range of Power Inductors



In addition to Würth Elektronik's five existing package sizes of WE-XHMI SMT power inductors there are now eight more packages. These compact yet very efficient inductors feature a current capacity up to 56 A saturation current and the ability to handle high transient current spikes. This makes them particularly suitable for use as DC/DC converters in power supplies, point-of-load converters and high-current filters, as well as in industrial computers, mainboards and graphics cards. The molded flat wire inductor, previously only available in the Power Magnetics product family, now also comes in 4020, 4030, 4040, 5020, 5030, 5050, 7030 and 7070 package sizes. The series is also available in smaller packages, and the 70xx sizes close a gap in the existing portfolio. The AEC-Q200-qualified WE-XHMI series inductors can be used at operating temperatures from -40 °C to +125 °C and cover an inductance range from 0.15 to 33 µH with currents up to 56 A.

www.we-online.com

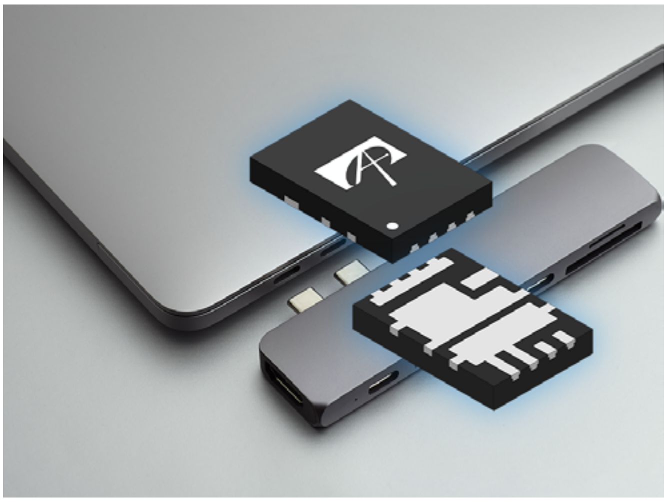
GaN IPM enables smaller, more energy-efficient high-voltage Motors

Texas Instruments introduced a 650V three-phase GaN IPM for 250W motor drive applications. The GaN IPM addresses many of the design and performance compromises engineers typically face when designing major home appliances and heating, ventilation and air-conditioning (HVAC) systems. The DRV7308 GaN IPM enables more than 99% inverter efficiency, optimized acoustic performance, reduced solution size and lower system costs. Supporting the trend of more compact home appliances, the DRV7308 helps engineers develop smaller motor drive systems. Enabled by GaN technology, the IPM delivers high power density in a 12mm-by-12mm package. Because of its high efficiency, the device eliminates the need for an external heatsink, resulting in motor drive inverter printed circuit board (PCB) size reduction of up to 55% compared to competing IPM solutions. The integration of a current sense amplifier, protection features and inverter stage further reduces solution size and cost.

www.ti.com

Half-Bridge MOSFET for DC-DC Applications

Alpha and Omega Semiconductor introduced its AONG36322 XSPairFET designed for space-constrained DC-DC applications.



The device features two 30V MOSFETs in a half-bridge configuration where the high-side and the low-side MOSFETs are in an asymmetric DFN3.5x5 XSPairFET package. This design allows the AONG36322 to replace an existing DFN5x6 asymmetric half-bridge MOSFET with an approximate 60 percent space-saving solution, thereby reducing the PCB footprint to further streamline the DC-DC architecture, resulting in a more efficient design. These benefits make the AONG36322 ideal for a new generation of smaller DC-DC buck converters in more compact applications such as point-of-load (POL) computing, USB hubs, and power banks. The AONG36322 is an extension to the AOS XSPairFET lineup, designed with the latest bottom-source packaging technology. Its integrated high-side and low-side MOSFETs feature 4.5 mOhms and 1.3 mOhms maximum on-resistance, respectively, where the low-side MOSFET source is connected directly to the exposed pad on the PCB to enhance thermal dissipation. A definite advantage of the state-of-the-art AONG36322 package design is that it delivers lower parasitic inductance, significantly reducing switch node ringing.

www.aosmd.com

AC/DC Power Supplies for AGV/AMR Battery Charging Stations

TTI – Europe is supporting the design and development of charging stations for industrial and service mobile robots with Advanced Energy’s Artesyn™ LCM series of single-output AC-DC power supplies. These robust and reliable units are tailored for fast and efficient charging of Automated Guided Vehicles (AGV) and Autonomous Mobile Robots (AMR) batteries in charging stations.

Within the LCM series there are five variants, ranging from 300 Watts to 3000 Watts. They offer a typical full-load efficiency of up to 93%, thereby reducing operating costs and improving thermal performance. Many models within this series do not require derating at low-line. The single output front-end units accept operating inputs between 90Vac and 264Vac for global use, and a wider 85Vac to 264Vac input range for the LCM300 & LCM600 series.

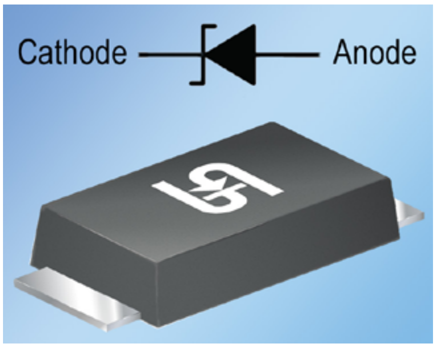
The LCM series is available with output voltages of 12V, 15V, 24V, 36V and 48V – the LCM1500 series is offered with an additional 28V output, with 18V and 72V for the LCM3000 series. All outputs are adjustable to a percentage of their nominal value, which means that any output voltage between 9.6 and 57.6V is available to accommodate non-standard system voltages. In addition, the ability to share current allows multiple power supplies to be connected in parallel for higher power applications.

www.ttieurope.com

Series of Ultra-Low Bias Current / High-Efficiency Zener Diodes

Taiwan Semiconductor announces its series of Zener diodes with a selection of devices providing regulated voltages from 1.8VDC to 39VDC, all with ultra-low bias current (IZT) of 50µA and maximum power dissipation (PD) of 500mW. These devices are ideal for applications where exceptionally low bias current is needed (to extend battery life), essential (for energy harvesting), or desirable (in lighting and IIoT) – while still providing uncompromised Zener regulation. The 39 individual Zener diodes in the series with part numbers ranging from MMSZ4668 to MMSZ41716 are all packaged in an industry-standard, low-profile, SOD-123 surface-mount package. With their low IZT, these devices are a straightforward upgrade to existing designs (without the need for PCB modifications), as well as for new designs.

www.taiwansemi.com



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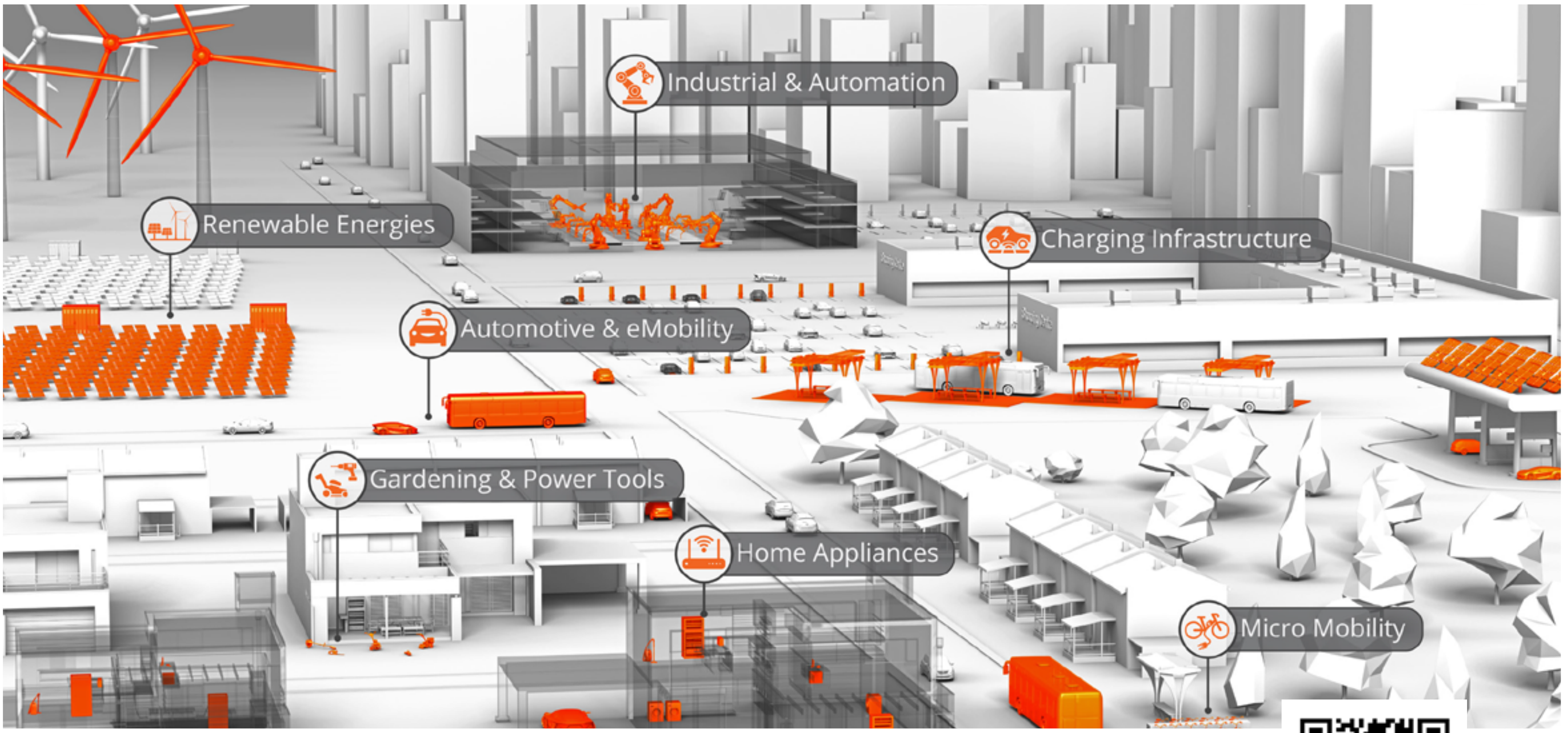

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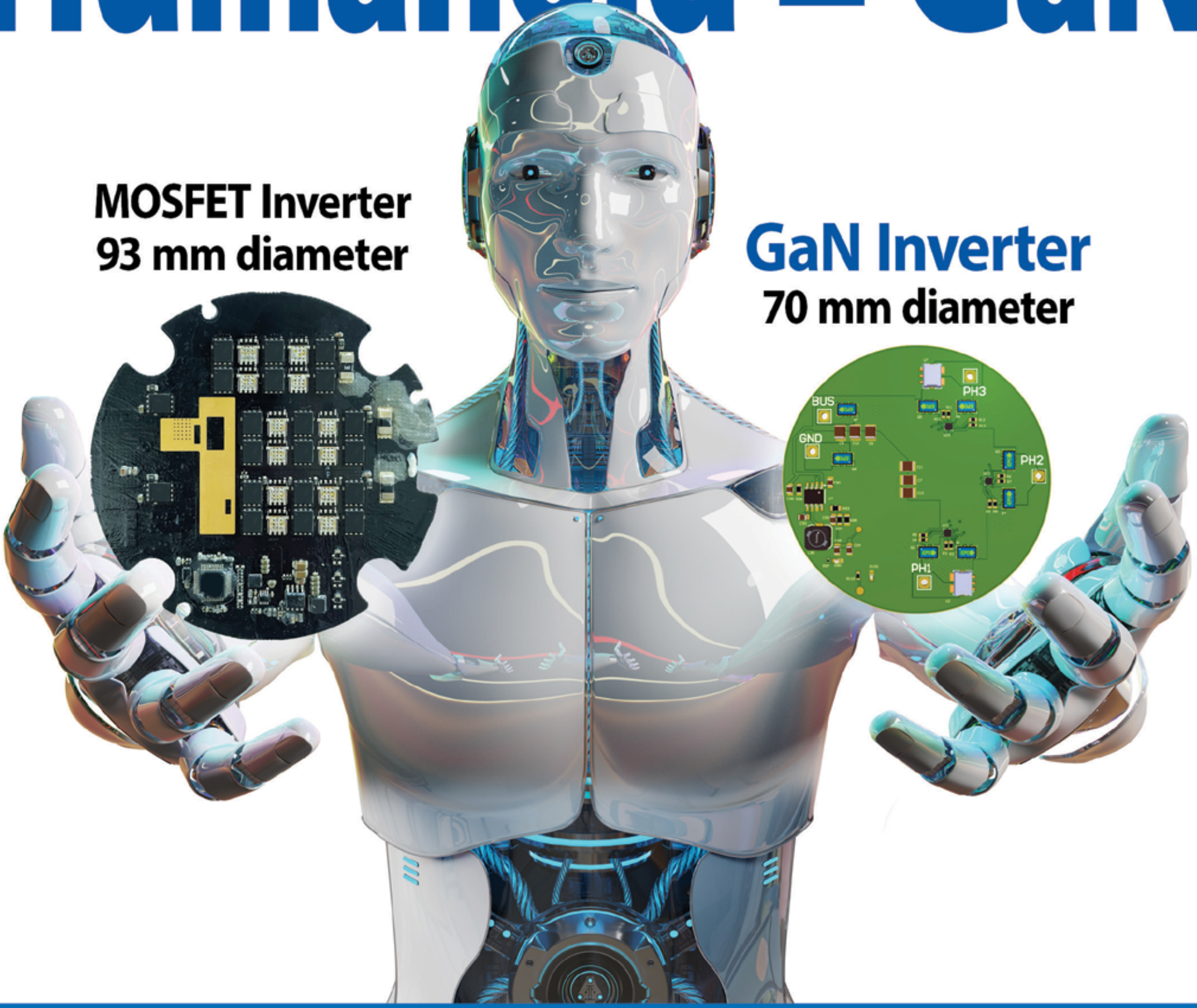
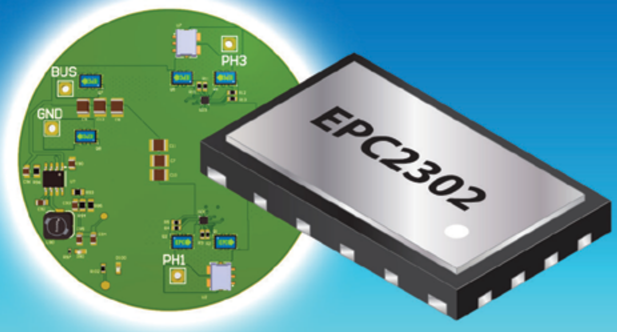

MOSFET Inverter
93 mm diameter
GaN Inverter
70 mm diameter
BUS
GND
PH3
PH2
PH1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