One Product Family Fits All: Gate Driver Solutions for Si, SiC, and GaN

Features and benefits of the new generation of dual-channel galvanically isolated gate driver ICs

This product family spans multiple under-voltage lockout (UVLO) variants, isolation levels, and package options to provide a comprehensive solution for various applications. The new portfolio combines robust isolation technology that meets the latest isolation standards with excellent electrical parameters and protection features to deliver high efficiency and reliable operation over a wide temperature range, extending the design's lifetime. These drivers can be used in a wide range of applications, including server and telecom SMPS, solar inverters and energy storage systems, motor drives and battery-powered applications, EV charging, and high-performance computing.

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Isolators are used today in a wide range of applications, from telecom and server switch-mode power supplies (SMPS) [1] to solar inverters, industrial AC motor drives, and EV charging. They are primarily used to offer the required protection from injury and electrical shock to the operators interfacing with HMI or connectors, as well as safeguard sensitive and expensive low-voltage components, such as controllers, against failures in the high-voltage power stage [2].

Often isolation is used to interrupt disruptive ground loops, eliminating displacement currents and high-frequency noise injected back into the control units.

Digital isolators and isolated gate driver ICs have become the technology of choice in the market thanks to their unquestionable benefits compared to traditional solutions such as pulse transformers [2] and optocouplers.

This article presents the features and benefits of the new EiceDRIVER™ 2EDi family of dual-channel isolated gate driver ICs. The new generation features DSO 14-pin packages for extended channel-to-channel creepage, dead-time, and shoot-through protection, faster start-up time, robust isolation technology meeting the latest isolation standards (VDE 0884-11, IEC 60747-17), as well as small LGA 4x4 packages enabling 36 percent space saving in low-voltage applications. With multiple under-voltage lockout (UVLO) variants, package options, and isolation levels, this family meets most design needs in several applications for the different switch technologies (see Table 1).

Isolation technology with excellent MFI and CMTI that meets the latest standard requirements

The new EiceDRIVER™ 2EDi generation exploits magnetic isolation with proven Infineon's Coreless Transformer (CT) technology. A repetitive working voltage of 1767 VRMS is ensured over 20 years

		Galvanic isolation			Output stages			Control inputs			
Package	Product name	Rating	Certification	CMTI	Sink/Source currents	UVLO on (nom.)	UVLO start-up	Channels	STP/DTC option	DIS/EN	Use case examples
WB DSO-16 300 mil DSO, 16-pin 2.5 mm Ch-Ch creepage	2EDS7165H	V_{ISO} = 5700 V_{RMS}	• UL1577 Single protection • EN 62368-1 Reinforced isolation • GB4843.1 Reinforced	150 V/ns	1 A / 2 A	4 V	5 µs	INA, INB	-	DIS	• Telecom and server SMPS, primary-side of HV DC-DC stage (e.g., LLC) with need of reinforced isolation • Solar microinverters and DC-DC power optimizers • EV off-board chargers
	2EDS8165H					8 V					
	2EDS8265H				5 A / 9 A	8 V					
	2EDS9265H					13 V					
WB DSO-14 300 mil DSO, 14-pin 3.3 mm Ch-Ch creepage	2EDR8259H	V_{ISO} = 5700 V_{RMS} V_{IOTM} = 8000 V_{pk} V_{IOSM} = 6875 V_{pk}	• VDE 0884-11 • IEC 60747-17 Reinforced isolation • UL1577 Single protection • EN 62368-1 Reinforced isolation • GB4943.1 Reinforced	150 V/ns	5 A / 9 A	8 V	2 µs	INA, INB	yes	DIS	
	2EDR7259X					4 V					
	2EDR8259X					8 V					
	2EDR9259X					15 V					
	2EDR8258X					8 V				EN	
	2EDR9258X					15 V					
	2EDR6258X					12 V					
NB DSO-16 150 mil DSO, 16-pin 2.5 mm Ch-Ch creepage	2EDF7175F	1500 V_{DC}	• functional	150 V/ns	1 A / 2 A	4 V	5 µs	INA, INB	-	DIS	• Telecom and server SMPS (e.g. totem-pole PFC, Vienna rectifier) • Low-voltage drives with ground bounce issues (LEVs, gardening tools, fork-lifters)
	2EDF7275F				5 A / 9 A	4 V					
	2EDF8275F					8 V					
	2EDF9275F					13 V					
NB DSO-14 150 mil DSO, 14-pin 3.3 mm Ch-Ch creepage	2EDB8259F	V_{ISO} = 3000 V_{RMS} V_{IOTM} = 4242 V_{pk} V_{IOSM} = 6000 V_{pk}	• UL1577 Single protection • GB4943.1 Basic	150 V/ns	5 A / 9 A	8 V	2 µs	INA, INB	yes	DIS	
	2EDB7259Y					4 V					
	2EDB8259Y					8 V					
	2EDB9259Y					15 V					
LGA 5x5 13-pin 1 mm Ch-Ch creepage	2EDF7275K	1500 V_{DC}	• functional	150 V/ns	5 A / 9 A	4 V	5 µs	INA, INB	-	DIS	• Non-isolated inverted buck-boost brick • Isolated dc-dc bricks • Low-voltage drives with ground bounce issues (LEVs, gardening tools, fork-lifters)
	2EDF7235K					4 V			DTC		
	2EDB7259K	V_{ISO} = 2500 V_{RMS} V_{IOTM} = 3535 V_{pk} V_{IOSM} = 6000 V_{pk}	• UL1577 Single protection • GB4943.1 Basic	150 V/ns	5 A / 9 A	4 V	2 µs	INA, INB	yes	DIS	
	2EDB8259K					8 V					
LGA 4x4 13-pin 0.75 mm Ch-Ch creepage	2EDB7259E	V_{ISO} = 2250 V_{RMS} V_{IOTM} = 3181 V_{pk} V_{IOSM} = 4000 V_{pk}				4 V					
	2EDB8259E					8 V					

EiceDRIVER™ 2EDi (Previous Gen.) EiceDRIVER™ 2EDi (New Gen.)

Table 1: Product overview of the new and previous generations of the EiceDRIVER™ 2EDi product family.

lifetime, fulfilling the time-dependent dielectric breakdown (TDDB) requirements of VDE 0884-11 and IEC 60747-17, the latest component standard for magnetic and capacitive couplers.

A proprietary double coil on-chip transformer also ensures high magnetic field immunity (MFI), fulfilling the most stringent test levels according to IEC 61000-4-8, IEC 61000-4-9, ISO 11452-8, and MIL-STD-461G-RS101 standards. It also provides an excellent common-mode transient immunity (CMTI) of more than 150 V/ns, fundamental for driving wide bandgap devices (WBG) such as SiC and GaN.

Robust insulation to electrical overstress (EOS) in the power stage
The robustness of the insulation in overstress scenarios is often of concern, particularly when it comes to potential failure and damage of the power stage across the reinforced isolation barrier.

Figure 1 depicts one of the worst-case scenarios, i.e., when the EiceDRIVER™ 2EDRx259X galvanic isolated gate drivers are used in an LLC topology, and one power switch fails with a gate-drain short circuit while the other is conducting.

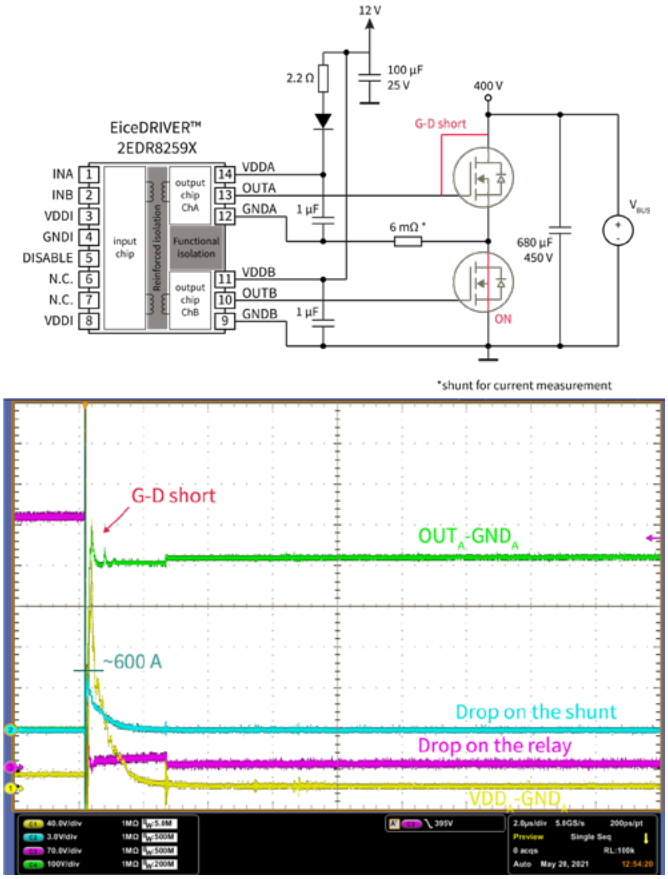

Figure 1: A critical EOS event in the power stage that could break the isolation barrier Despite the high energy injected into the driver (up to 600 A current flowing into OUT_A until bond-wire evaporation and package explosion), the EiceDRIVER™ 2EDRx259H guarantees the fully reinforced isolation integrity.

Without a protection diode between the driver output and its ground, a significant amount of energy is transferred from the bulk capacitor (680 µF in this example) directly into the driver leading to electrical failure of the output chip ChA and package destruction with open bond wires. The EiceDRIVER™ 2EDRx259X ensures total isolation even after high electrical overstress, thanks to the robust insulation built on the primary-side chip. Competitors 2 and 3, using a capacitive isolation technology, fail the Hi-Pot test after EOS stress.

Table 2 shows the summary results of the Hi-Pot test at rated V_{ISO} voltage after EOS stress.

Product	Pass high-voltage Hi-Pot test* after EOS stress
2EDRx259X/H	Yes
Competitor 1	Yes
Competitor 2	No
Competitor 3	No

*V_{ISO} = 5700 V_{RMS} for t = 60 sec, V_{ISO} = 5000 V_{RMS} for competitors 1, 2 as per datasheet specification

Table 2: Isolation robustness against output-side EOS after Hi-Pot test at rated V_{ISO}.

Fast UVLO timing

A bootstrap circuit is often used to supply the high-side MOSFET due to its simplicity and low cost. However, it can hide several complications because, by nature, the bootstrap supply and the low-side supply are unavailable during start-up. Consequently, the supply voltage in the high-side channel becomes available after some delay, depending on the size of the bootstrap capacitor and resistor.

Many gate driver ICs on the market show a UVLO start-up time in tens of µs (left of Figure 2), meaning several high-side pulses are skipped while the low-side MOSFET turns on and off in normal operation.

This can lead to several consequences, e.g., it can create unbalance in the two resonant capacitors of an LLC topology. If not properly controlled, this can generate severe hard commutation issues. On top of that, it can create voltage asymmetry on the main transformer with a saturation of the core. The new EiceDRIVER™ 2EDi generation features an industry benchmark UVLO start-up time lower than 2 µs ensuring high-side activation in less than one pulse (Figure 2).

Figure 2: UVLO start-up time of a competitor driver with slow bootstrap channel activation (top) vs. the new EiceDRIVER™ 2EDi with the fastest output-side activation time (bottom).

Fast active output clamping to avoid shoot-through

Another potential issue hidden in the bootstrap system can arise when induced noise on the high-side gate is not effectively clamped by the driver that is still "inactive," being the charging bootstrap supply below the UVLO level.

One example is the start-up in LLC with split resonant capacitors (see Figure 3). If no special start-up sequence is considered, the high-side MOSFET is OFF until (and after a certain delay) the bootstrap supply approaches the UVLO, creating voltage unbalance on the resonant capacitor and an unwanted change of the switching node (in green). Each negative dV/dt of the switching node charges the gate of the high-side power switch (in magenta) via the Miller effect.

The new EiceDRIVER™ 2EDi generation includes a special active clamping circuit to quickly clamp the output noise even if the channel is "inactive" (output supply below UVLO), thus avoiding dangerous shoot-through events, as shown in the right-hand side measurements of Figure 3.

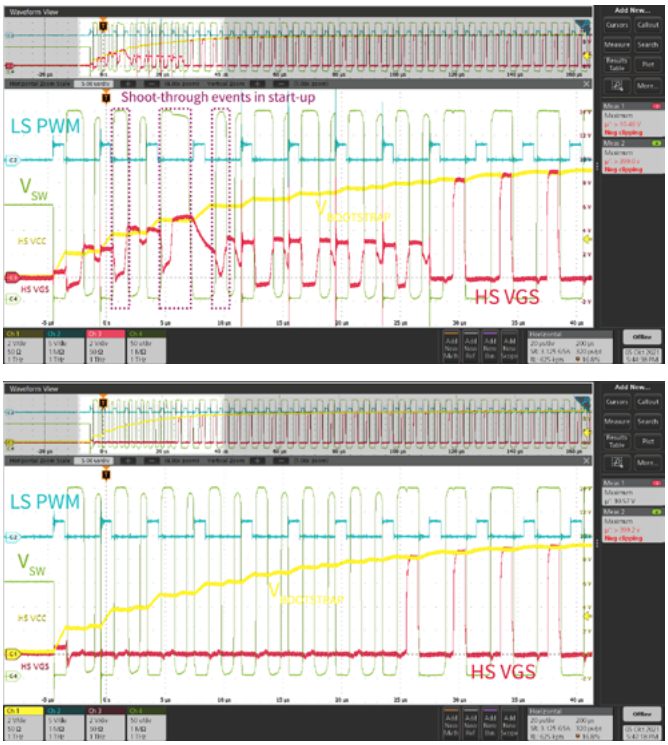

Figure 3: A critical shoot-through when using a driver with a slow output clamping for supply below UVLO (top). The outperforming clamping behavior of the new generation of EiceDRIVER™ 2EDi gate driver ICs (bottom). Both measurements are related to a start-up condition in an LLC circuit with split resonant capacitors and with bootstrap.

Accurate timing and Dead-time control (DTC)

The new EiceDRIVER™ 2EDi generation includes features that fulfill the needs of fast-switching applications employing WBG devices. Excellent propagation delay matching and dead-time accuracy (see Table 3) ensure perfect timing synchronization of the gate signals (e.g., in diagonal driving) and dead-time optimization with huge benefits on system reliability and efficiency performance.

Feature	Values
Part-to-part propagation delay turn-on	6 ns (max)
Part-to-part propagation delay turn-off	8 ns (max)
Ch A-to-Ch B turn-on propagation delay mismatch	-4 ns – 4 ns
Ch A-to-Ch B turn-off propagation delay mismatch	-5.5 ns – 3 ns
Channel turn-off to turn-on prop. delay mismatch	-5 ns – 1 ns
Pulse width distortion	-5 ns – 5.5 ns

Table 3: Tight timing specifications enable WBG driving.

Furthermore, important second-level safety mechanisms are configurable shoot-through protection (STP) and dead-time control (DTC) built into the gate driver IC hardware.

The EVAL_2EDB_HB_GaN evaluation board (Figure 4) combines an EiceDRIVER™ 2EDB8259Y dual-channel isolated gate driver with Infineon's discrete GaN HEMTs. This board allows testing in different operating modes and with different driving supply approaches (unipolar or bipolar, isolated or non-isolated with bootstrap).

The test results obtained with gate injection transistor (GIT) HEMTs demonstrate a reliable operation at MHz and kW range [3]. The board also includes a flexible bias supply configurable for bipolar or unipolar operation with different voltage levels and an option for one percent voltage regulation, which is particularly important while driving Schottky gate (SG) GaN HEMTs. Detailed information about a universal gate driving circuit for both 650 V GIT and SG GaN HEMTs is described in [4].

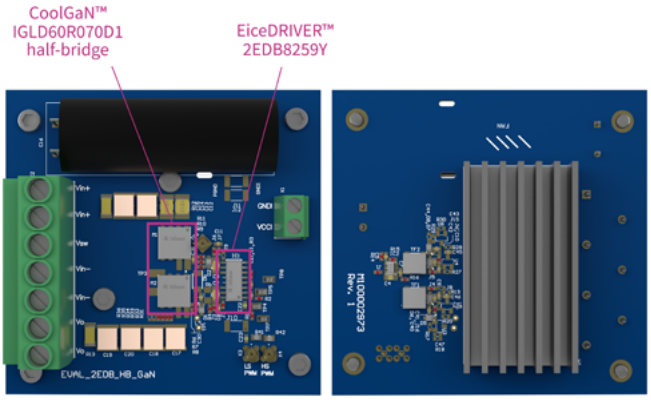

Figure 4: EVAL_2EDB_HB_GaN CoolGaN™ GIT HEMT half-bridge evaluation board.

Conclusion

The new EiceDRIVER™ 2EDi generation combines the benefit of robust isolation technology with outstanding electrical parameters. The features of this new product family can support system requirements to achieve high efficiency and reliable operation over a wide temperature range and with a longer lifetime.

Infineon's broad product portfolio includes different packages and isolation ratings, providing a comprehensive offering adapted to the needs of different application use cases and topologies.

For a deeper understanding of the new EiceDRIVER™ 2EDi generation, we invite you to delve into the wealth of information provided in the dedicated application notes [3] and product webpage. Scan the QR code below to find out more.

References

1. Infineon Technologies AG, "Using the EiceDRIVER™ 2EDi product family of dual-channel functional and reinforced isolated MOSFET gate drivers," Application Note v4.0, March 2022, AN_1805_PL52_1806_095202, March 2022, [Online] https://www.infineon.com/cms/en/product/power/gate-driver-ics/dual-channel-isolated-gate-driver-eicedriver-2edi/#!?fileId=5546d46267354aa001675a431da84a41
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4. C. Menditti Matrisciano, A. Laneve, and D. Varajao, "Universal Isolated Gate Driving Platform for 650 V GaN HEMTs Half-Bridge with Dead-Time Control and Integrated Bias Supply," PCIM Europe 2023; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nuremberg, Germany, 2023, pp. 1-9.

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