Advancements in USB Power Delivery: GaN Technology for Efficiency and High-Power Density

The first Universal Serial Bus (USB) specification, released in 1996, aimed to standardize power delivery and connectivity in computing and telecommunication industries [1]. Initially supporting a 5 V power bus with up to 5 A of current (25 W) and maximum data transfer rates of 12 Mbit/s, USB has evolved significantly due to the proliferation of electronic devices, leading to a demand for higher power capabilities.

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Today, USB systems are used not only for data transfer and powering low consumption devices; they have become the solution for battery charging as well. Such evolution has been coordinated by the multiple revisions of the USB specification since 1996, with the latest major milestone being the USB Power Delivery (USB PD) Revision 3.1 update in 2021 [2]. This, combined with an upgrade to the USB connector, from the original Type-A to the newer Type-C, has set the path for over 10 Gbit/s data transfer and up to 240 W of power delivery. As shown in figure 1, the new USB PD 3.1 specification establishes a series of bus voltages to cover the different power levels. A maximum of 5 A over the cable and connector sets the power delivery limit at each voltage, thus increasing the voltage level remains the only way to increase power transfer.

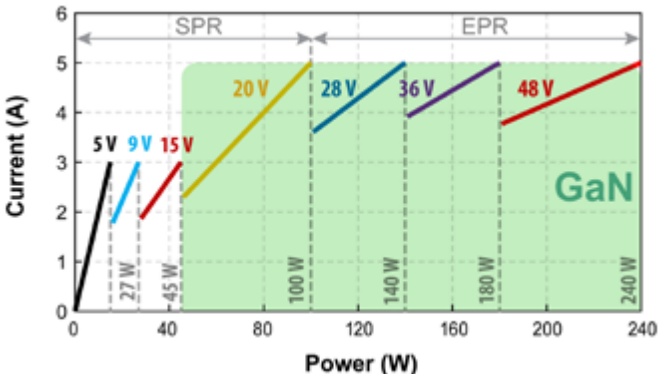

Figure 1: USB PD 3.1 specification: Power and current levels and corresponding bus voltages

Silicon-based products have been widely used to cover the Standard Power Range (SPR) due to the possibility of monolithic integration of the protocol IC, controller, and power devices, leading to reduced cost, complexity, and size [3]. However, silicon alone cannot achieve this level of integration, or the high efficiency needed to realize high power densities and low profiles over the entire Extended Power Range (EPR). Here is where GaN technology offers unmatched performance. The latest generation of 100V-rated eGaN® transistors have over 5x lower $R_{DS(on)}$*Q_{OSS} and 2.5x lower $R_{DS(on)}$*Q_G compared of their silicon counterparts [4]. Hence, converters can be made simultaneously more efficient and smaller.

Figure 2 shows simplified block diagrams of USB PD 3.1 systems where GaN is used in the power stage to cover the entire EPR. As shown, GaN technology can be deployed on both sides of the cable to create small and efficient USB PD solutions. First, on one side, a multiple port charger is pictured, where each port uses a regulated buck converter, fed from a common input, to provide the desired voltage on the USB cable. On the other side of the cable, GaN is featured in a buck converter to step the voltage down to 12 V or 20 V. This second application can be found in most laptops or other battery-power devices where the output voltage is set by the device's battery voltage.

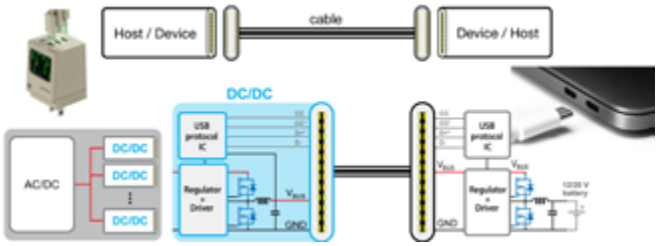

Figure 2: USB PD block diagrams using GaN devices

This article presents an example to illustrate the advantages of GaN technology for USB PD applications. It is based on EPC's recently released reference design, EPC9195 [6], which could be used as a battery charger. The design features a regulated buck converter using GaN transistors in combination with an analog controller [5] and it demonstrates how to unlock very high-power densities while delivering up to 240 W to a load from a 48 V bus in a very simple implementation. The article continues with a brief overview of the converter and a description of its key components, followed by the design validation results.

Converter Overview

The EPC9195 design utilizes a compact and efficient synchronous buck converter with a wide input voltage range from 20 V to 60 V capable of delivering up to 240 W to a regulated 13 V output, making it ideal for battery charger in a USB PD 3.1 compatible device.

The converter occupies a very small functional circuit area of 1025 mm^2 as shown in figure 3. Despite its small size, the converter achieves a remarkable peak efficiency of 98%, operating at a switching frequency of 750 kHz. This high frequency allows for a reduction in the size of passive components, including the inductor and input/output capacitors. A 1.5 µH molded inductor with low

DCR and only 3.5 mm height complies with the stringent profile restrictions of modern computers. The key to this high efficiency and power density lies in the use of two latest-generation 100 V rated, 4.2 mΩ, EPC2619 eGaN transistors [7], configured in a half bridge.

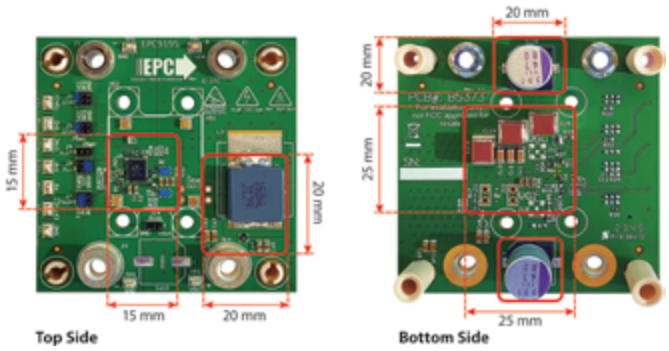

Figure 3: Shows the functional circuit area of EPC9195 Board

The GaN devices are paired with the LTC7891 IC from Analog Devices, which integrates both the buck controller and the half-bridge gate driver onto a single chip. The result is a very simple and compact solution with a minimal component count. For more details, refer to the functional block diagram of the EPC9195 design provided in Figure 4.

Power Transistor

In the EPC9195, two EPC2619 GaN transistors are configured in a half-bridge configuration. These 100 V rated transistors boast superior performance and power density to competing silicon FETs with similar voltage ratings. With a footprint of only 2.5 mm x 1.5 mm, they offer a maximum $R_{DS(on)}$ of 4.2 mΩ and the lowest commercially available $R_{DS(on)}$*C_{OSS} at this voltage. Low $R_{DS(on)}$ is crucial to minimize conduction losses while low C_{OSS} helps in reducing the transition times and minimizes switching losses. The combination of these factors leads to a significant improvement in overall efficiency and impressive power density.

Controller

The EPC9195 employs the LTC7891, a synchronous step-down peak current mode controller from Analog Devices. Operating at a fixed frequency of 750 kHz (configurable up to 3 MHz), the LTC7891 offers adjustable dead time between switching the high-side (Q_1) and low-side FETs (Q_2). Dead time refers to the brief period when both the high-side and low-side FETs are off during switching cycles. Users can adjust this parameter to 10 ns, 20 ns, or near zero. This feature is particularly beneficial for GaN FETs, which have inherently higher reverse conduction voltage compared to traditional MOSFETs. Minimizing dead time to near zero reduces energy losses that occur when the lower FET (Q_2) conducts reverse current, resulting in significantly improved efficiency while maintaining the advantages of GaN FETs.

The EPC9195 also offers adjustable inductor current limit to ensure the current delivered through USB 3.1 PD does not exceed 5 A or the maximum allowed power, ensuring compliance with USB specifications. Users can set the peak current threshold to 25 mV, 50 mV, or 75 mV to achieve the desired level of protection. For more information, please refer to [5]. Additionally, the controller offers three light-load power-saving modes: bursting mode, pulse-skipping mode, and forced continuous mode. These power saving modes help maintain high efficiency over the entire load range. Each mode provides a trade-off between efficiency and output voltage ripple. By selecting the appropriate saving mode, the user can achieve the balance performance for the specific requirement.

- Pulse-skipping mode: This mode balances efficiency with a lower level of output voltage ripple compared to bursting mode.
- Bursting mode: This mode prioritizes efficiency, but it comes with the highest output voltage ripple.
- Forced continuous mode: This mode delivers the lowest output voltage ripple, but at the expense of lowest efficiency.

Additionally, users can enable spread spectrum mode which is particularly beneficial for applications where electromagnetic interference (EMI) is a concern.

In summary, the EPC9195 with its cutting-edge design using EPC2619 GaN FETs enables a highly efficient and highest power density converter possible. This combination of efficiency and compactness makes the EPC9195 ideal for integration into portable devices. Furthermore, its compatibility with USB PD 3.1 standards makes it a perfect solution for powering next-generation electronic devices from USB PD 3.1.

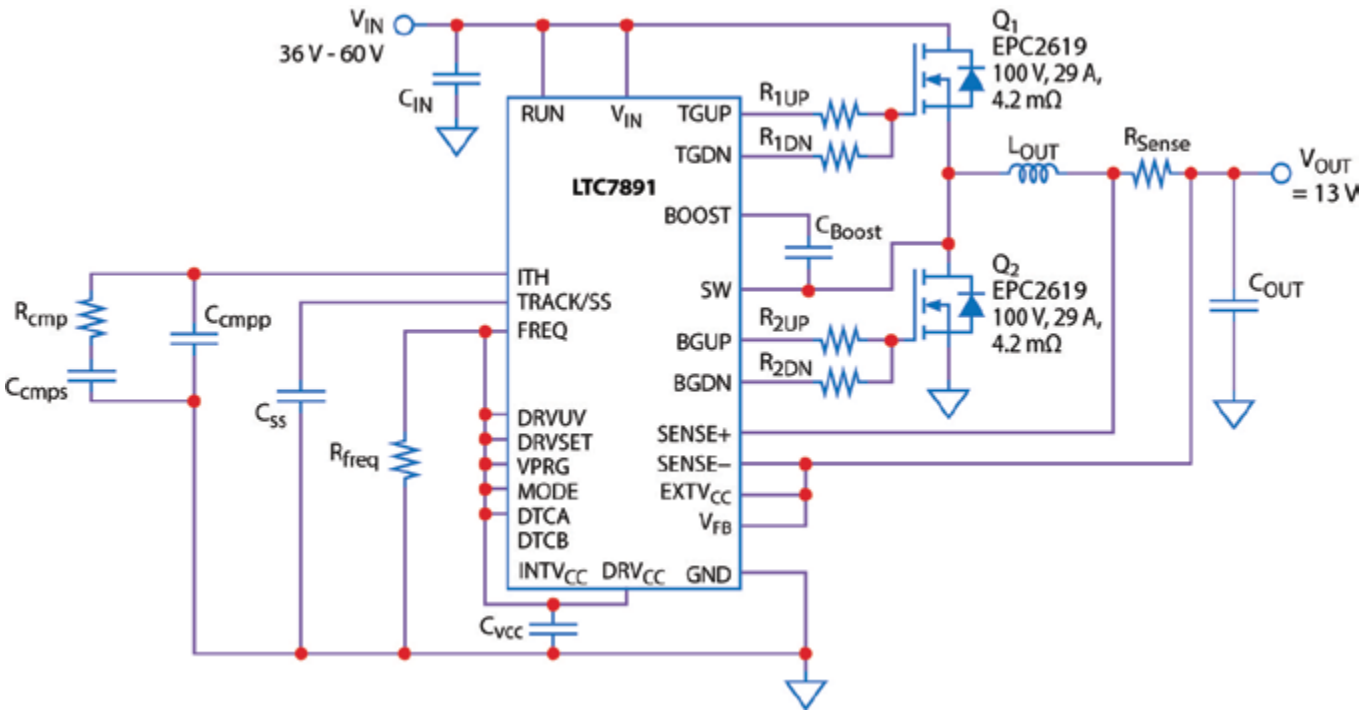

Figure 4: Diagram overview of the EPC9195 Evaluation Board

Design Validation Results

Electrical Performance

Figures 5 and 6 illustrate the measured efficiency and power losses of the EPC9195 under various supply voltages and output currents. The output current was swept for each input voltage until the input current reached 5.2 A, which corresponds to the maximum power allowed by the USB PD 3.1 specification. (refer to figure 1).

Figure 7 shows the voltage waveform at the switch node pin (drain of Q_2) referenced to ground. The waveform depicts the switch node voltage at an input voltage of 28 V and an output power of 140 W, highlighting the converter's impressive characteristic of switch node rise times below 2 ns, as well as the near- zero dead time feature.

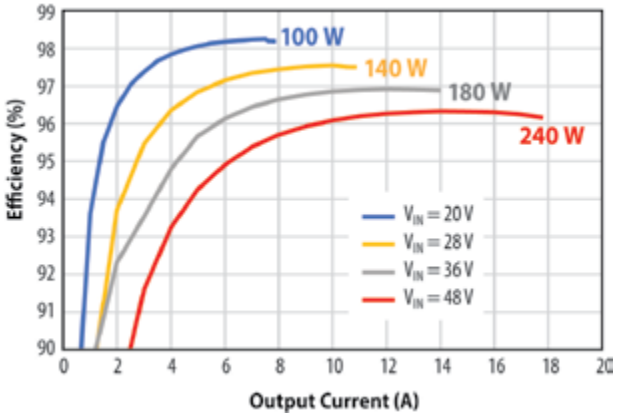

Figure 5: The efficiency graph at various input voltages and output currents

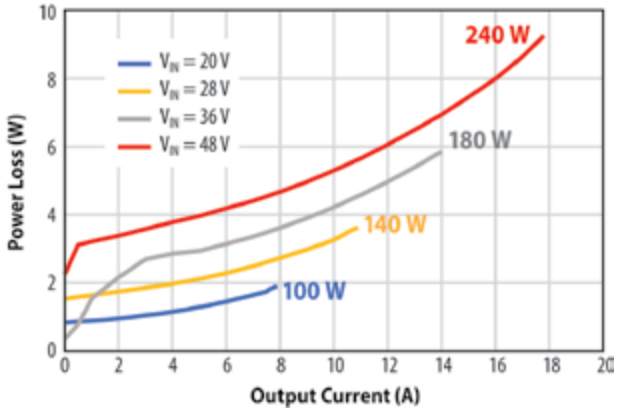

Figure 6: The power loss graph at various input voltages and output currents

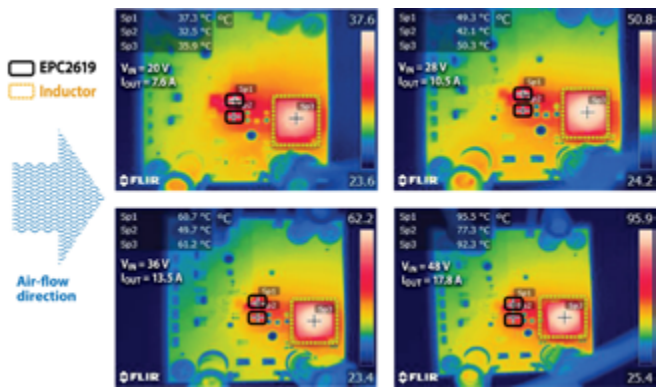

Figure 8: Steady state measured thermal image of the EPC9195 operating with different input voltages, 5 A input curent, 13 V output, 400 LFM airflow and no heatsink attached

Thermal Performance

Figure 8 displays the measured thermal performance of the EPC9195 operating with input voltages of 20 V, 28 V, 36 V, and 48 V. The output was set to 13 V and delivered with an input current of 5 A, without a heatsink installed and with 400 LFM airflow.

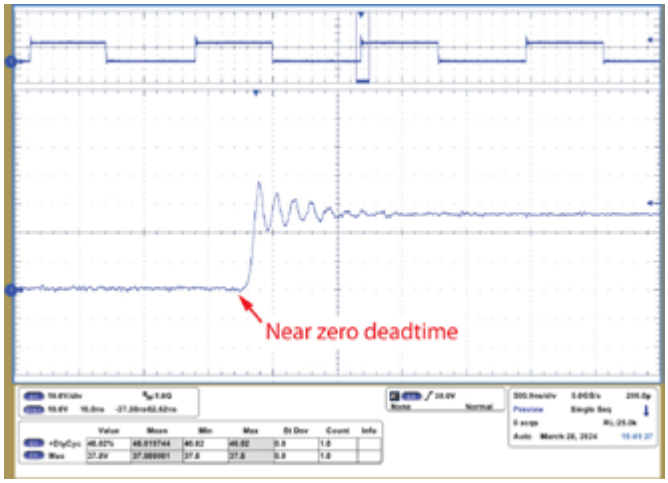

Figure 7: Zoom in view of switch node waveform the input voltage of 28 V and output power of 240 W

Summary

The article discusses the evolution of USB technology, particularly focusing on the USB Power Delivery (USB PD) 3.1 specification and the role of GaN technology in enhancing power delivery efficiency and density. It highlights the challenges posed by the increasing power demands of modern electronic devices and how GaN technology addresses these challenges. The article presents a case study of EPC9195, a reference design for a high-power density USB PD charger, showcasing the advantages of GaN transistors and an analog controller in achieving high efficiency and compactness. Experimental results demonstrate the performance and efficiency of the design, making it a suitable solution for next-generation electronic devices requiring USB PD 3.1 compatibility.

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