ISSN: 1863-5598

ZKZ 64717
02–24

Bodo´s Power Systems®

Electronics in Motion and Conversion

February 2024

PULSED INDUCTANCE MEASUREMENT

POWER CHOKE TESTER DPG10/20 SERIES

Inductance measurement from 0.1 A to 10 kA

KEY FEATURES

Measurement of the
- **Incremental inductance** $L_{inc}(i)$ and $L_{inc}(\int Udt)$
- **Secant inductance** $L_{sec}(i)$ and $L_{sec}(\int Udt)$
- **Flux linkage** $\psi(i)$
- **Magnetic co-energy** $W_{co}(i)$
- **Flux density** B(i)
- **DC resistance**

Also suitable for 3-phase inductors

APPLICATIONS

Suitable for all inductive components from **small SMD inductors** to **very large power reactors in the MVA range**
- **Development, research** and **quality inspection**
- **Routine tests** of small batch series and mass production

KEY BENEFITS

- Very **easy and fast** measurement
- **Lightweight, small and affordable price-point** despite of the high measuring current up to 10000A
- **High sample rate and very wide pulse width range** => suitable for all core materials

AVAILABLE MODELS

Model	max. test current	max. pulse energy
DPG10-100B	0.1 to 100A	1350J
DPG10-1000B	1 to 1000A	1350J
DPG10-2000B	2 to 2000A	1350J new model
DPG10-2000B/E	2 to 2000A	2750J new model
DPG10-3000B/E	3 to 3000A	2750J
DPG10-4000B/F	4 to 4000A	8000J
DPG20-10000B/G	10 to 10000A	15000J

Technological leader in pulsed inductance measurement for 20 years

www.ed-k.de

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Electronics in Motion and Conversion

February 2024

Improved application efficiency with novel MOSFET technology

infineon

OptiMOS™ 6

Revolutionizing power MOSFET technology – Infineon's novel needle trench design

Infineon has begun a new chapter in the evolution of power MOSFETs. The latest OptiMOS™ 6 power MOSFET technology utilizes a novel needle trench cell design, pioneering a full three-dimensional charge compensation principle which brings improvements in the on-state resistance. At the same time, the completely redesigned gate module leads to an outstanding reduction of gate charges, ultimately enabling high-frequency operation.

Key features

- Offers extended SOA and ruggedness
- Optimizes the switching behavior of the device
- Reduces on-state resistance by up to 30 percent
- Reduces gate- and gate-drain charges by up to 40 percent
- Provides enhanced system efficiency and power density in various applications

By improving the $R_{DS(ON)}$ and switching parameters, the needle trench technology provides a significant improvement across all figures of merit. It enables high-frequency operation, making these devices ideal for telecom and datacenter applications.

For more details scan the QR code.

Content

Supporters & Friends

WÜRTH ELEKTRONIK MORE THAN YOU EXPECT

COMPACT. EFFICIENT. SILENT.

INFUSED BY INNOVATION.

WE meet @ APEC

State of the Art Power Modules

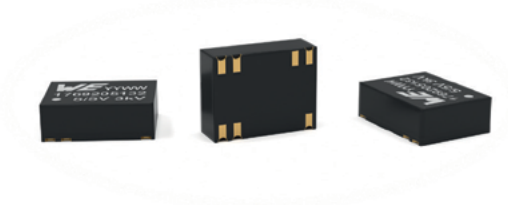
The MagI³C FIMM Fixed Isolated MicroModule series combines the features of an isolated power module with those of a classic MicroModule. It is realized in an LGA-7 housing and impresses with its miniaturized dimensions. The 1 W output power can be provided up to an ambient temperature of TA = 100 °C without derating. Features like continuous short circuit protection (SCP) and dynamic power boost up to 300 mA for 500 ms ensures a robust performance for industrial applications. The module complies with EN55032 (CISPR-32) class B conducted and radiated emissions standard and requieres no external components for operation.

www.we-online.com/INFUSEDBYINNOVATION

#FIMM

Highlights

- LGA-7 housing (9 mm x 7 mm x 3.1 mm)
- Ambient temp range from -40 °C to +125 °C
- Typ. 8 pF parasitic coupling capacitance
- Efficiency up to 91 %
- Certified according UL62368-1
- Dynamic and static power boost



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Hello, here I am!

Only some of you already had a chat with me at Bodo's WBG event last December. My name is Alfred Vollmer and I'm the new guy in the editorial team of Bodo's Power, but I am not new to the industry at all; I even wrote a viewpoint like this before: it was for the June 2014 edition of Bodo's Power as a guest editorial. Like the vast majority of you I am an electrical engineer (German degree: Dipl.-Ing.) which means that I am somewhat tech-savvy in my daily life. You should have seen how proud I was in the early eighties when my first LDO-based "fully stabilized" power supply worked. And I was even prouder after setting up my very first switchmode power supply (SMPS) for a commercial control unit in 1985 that I optimized e. g. in terms of diode costs. But this is old days' stuff.

Immediately after graduation in the mid-eighties I started my very first job writing about semiconductors for a German publication. In these days there were only very few power semiconductor applications, and motor control was very different from today's energy-efficient inverter applications. However, with the advent of more affordable and more attractive power semiconductors I have been able to witness the success and conquest of new power semiconductor generations and technologies. I have always listened from row #1 because, being an electronics journalist for more than 30 years, also meant getting the information first-hand and talking to the experts quite frequently.

Today, wide bandgap (WBG) semiconductors based on Silicon Carbide (SiC) or Gallium Nitride (GaN) are THE hot products in our industry but definitely not the universal remedy for all application hiccups or challenges. SiC and GaN devices are often more expensive when you only look at the pure high-power semiconductor, however, from a system level perspective WBG semiconductors offer many advantages and they even enable some applications that haven't been economically or technically feasible before. I personally consider this view at the system level design to be one of the most important challenges of design engineers. This is why I will always keep the overall system implications in focus even while writing/reporting about very deep-diving technology and application-oriented details.

Please send me an e-mail to alfred@bodospower.com and tell me what you really want to read about! Bodo's Power is here to help you to solve your power design problem, and together with Bodo and Holger I will do my very best to serve to you exactly the information you need – promised!

Bodo's magazine is delivered by postal service to all places in the world. It is the only magazine that spreads technical information on power electronics globally. We have EETech as a partner serving our clients in North America. If you speak the language, or just want to have a look, don't miss our Chinese version at bodospowerchina.com. An archive of our magazine with every single issue is available for free at our website bodospower.com.

My Green Power Tip of the Month:
Unplug AC adaptors when not in use – especially when they still feel warm because their ohmic resistance is too high. Perhaps it is time to get rid of these old chargers, disposing of them properly, even though this creates new electronic waste. The new generation of (fast) USB-C charging devices will help your decision.

Alfred Vollmer

Events

Advancements in Thermal Management 2024
Orlando, FL, USA February 14
www.thermalconference.com

IEEE ISSCC 2024
San Francisco, CA, USA February 18 – 22
www.isscc.org

The Smarter E India 2024
Gandhinagar, India February 21 – 23
www.thesmartere.in

APEC 2024
Long Beach, CA, USA February 25 – 29
www.apec-conf.org

EMV 2024
Cologne, Germany March 12 – 14
https://emv.mesago.com

CIPS 2024
Dusseldorf, Germany March 12 – 14
www.cips.eu

PLECS Conference 2024
Zurich. Switzerland March 12 – 13
https://plexim.com/events/seminars/2215

AMPER 2024
Brno, Czech Republic March 19 – 21
www.amper.cz

SEMICON China 2024
Shanghai, China March 20 – 22
www.semiconchina.org

Need a low range current sensor that offers high resolution?

HMSR DA series

The new HMSR DA family of integrated current sensors designed by LEM is the first to include an ADC with a sigma-delta bitstream digital output.

High-resolution, ease-of-use and an output that follows the increase or decrease of the input with configurable delay, makes it easier to develop a wealth of control systems.

This makes the HMSR DA the first choice for standalone servo drives, robotics, high precision machines, automated guided vehicles (AGVs) and CNC machine tools.

www.lem.com

- **Current range 6-30 A_{RMS} continuous at 125°C**
- **75 A peak current**
- **Digital bitstream output with 10 MHz clock**
- **More cost-effective and compact than discrete alternatives**

LEM

Life Energy Motion

Michael Sleven Appointed Vice President Sales Europe

Sanan Semiconductor has announced a major step towards strengthening its position in innovative, high-quality solutions with wide bandgap semiconductor materials with the appointment of renowned power electronic engineer Michael Sleven as Vice President Sales Europe. Anticipating significant growth in the European market, Sanan Semiconductor has chosen to boost its top management team with the recruitment of a specialist in the power electronics community who has over 25 years' experience in the sector in various management positions.

Michael joins the company after his time with LEM Europe GmbH as Managing Director and Head of Sales. Before that, Michael was responsible for business development and sales for power semiconductors (based on Silicon IGBTs and SiC MOSFETs) at Hitachi Europe. The main market sector here was automotive and industry applications in Europe. Michael also spent more than a decade at Infineon AG in a number of key positions, including Head of R&D High Power Semiconductor Module Development.

The appointment comes at a time when Sanan Semiconductor is undertaking a recruitment drive in its SiC and GaN team in Europe with over 10 positions available. The company is looking for sales managers, field application engineers, R&D engineers and customer service team member. The recruits will also support the development of innovative wide bandgap semiconductors that meet the increasing electrification needs of the automotive industry, as well as power conversion in green energy applications.

www.sanan-semiconductor.com

Renesas to Acquire Transphorm: Expanding its Power Portfolio with GaN Technology

Renesas Electronics and Transphorm announced that they have entered into a definitive agreement pursuant to which a subsidiary of Renesas will acquire all outstanding shares of Transphorm's common stock. The transaction values Transphorm at approximately $339 million. The acquisition will provide Renesas with in-house GaN technology, which is described by Renesas to be "a key next-generation material for power semiconductors, expanding its reach into fast-growing markets such as EVs, computing (data centers, AI, infrastructure), renewable energy, industrial power conversion and fast chargers/adapters". Renesas claims that demand for GaN is predicted to grow by more than 50 percent annually. Renesas will implement Transphorm's auto-qualified GaN technology to develop new enhanced power solution offerings, such as X-in-1 powertrain solutions for EVs, along with computing, energy, industrial and consumer applications. The transaction is expected to close in the second half of calendar year 2024, subject to Transphorm stockholder approval, required regulatory clearances and the satisfaction of other customary closing conditions. In other news Renesas had already announced the establishment of an in-house SiC production line, supported by a 10 year SiC wafer supply agreement.

www.renesas.com

Strengthening the Scandinavian Presence

With the establishment of Würth Elektronik Danmark A/S, customers from Denmark, Greenland and the Faroe Islands now have a direct point of contact for their electronic and electromechanical component needs. Previously, these markets were also served by the Swedish subsidiary.

Würth Elektronik Danmark A/S is based in the north of Aarhus. A team headed by CEO Ole Sanggaard Knudsen, Finance Manager Gunhild Nors and Office Manager Claire Boelstoft is being set up there to provide even better support for the Danish electronics industry.

www.we-online.com

We wish to issue a formal retraction regarding the January 2024 issue in which the power module image on page 16 was incorrectly labelled. We want to clarify that there is no connection between the power module and the company ABB. After thorough review, we acknowledge the error and sincerely apologise for any confusion caused.

Watch ROHM's
Stories of Manufacturing

ROHM
SEMICONDUCTOR

POWER THE FUTURE
ROHM'S GEN 4 SiC POWER DEVICES

As a technology leader ROHM is contributing to the realization of a sustainable society by focusing on the development of low carbon technologies for automotive and industrial applications through power solutions centered on SiC Technology. With an in-house vertically integrated manufacturing system, ROHM provides high quality products and stable supply to the market. Take the next development step with our Generation 4 SiC power device solutions.

Industry-leading low ON resistance

Reduced ON resistance by 40% compared to previous generation without sacrificing short-circuit ruggedness.

Minimizes switching loss

50% lower switching loss over previous generation by significantly reducing the gate-drain capacitance.

Supports 15V Gate-Source voltage

A more flexible gate voltage range 15 -18V, enabling to design a gate drive circuit that can also be used for IGBTs.

www.rohm.com

Donation for Educational Initiative

Vincotech is carrying on its holiday tradition of donating to a good cause in lieu of sending gifts to customers. The company's partner in philanthropy, Plan International Germany, is to receive a €12,000 grant from Vincotech on behalf of its workforce and customers. The money will fund a drive to further girls' education in Malawi.

This Plan International Germany project addresses the educational challenges faced by young people in Malawi, particularly girls in impoverished rural areas. Much of Malawi's population – 70 percent – lives below the poverty line. With traditional role models still holding sway, just 21 percent of girls finish secondary school. Plan International Germany aims to boost attendance and graduation rates by providing scholarships, improving sanitary facilities, and creating a mentoring program to guide and support girls on their way through school.

www.vincotech.com

Peter Henry Appointed to Board of Directors

Analog Devices announced that its Board of Directors has appointed Dr. Peter B. Henry as an independent director and member of the Board's Audit Committee effective December 5, 2023. Dr. Henry is currently the Class of 1984 Senior Fellow at the Hoover Institution and Senior Fellow at the Freeman Spogli Institute for International Studies, both at Stanford University. He is also Dean Emeritus of New York University's Leonard N. Stern School of Business. His appointment expands ADI's Board to 13 members. Dr. Henry also leads the Ph.D. Excellence Initiative (PhDEI), a post-baccalaureate program designed to address underrepresentation in economics by mentoring exceptional students from underrepresented backgrounds interested in pursuing doctoral studies in the field. For his founding and leadership of the PhDEI, Dr. Henry received the 2022 Impactful Mentoring Award from the American Economic Association.

Dr. Henry received a bachelor's degree in economics from the University of North Carolina at Chapel Hill, a bachelor's degree in mathematics from Oxford University where he was a Rhodes Scholar, and a Ph.D. in economics from the Massachusetts Institute of Technology.

www.analog.com

Collaboration on Magnetic Components for Converters

ITG Electronics has announced a collaboration with Renesas Electronics to develop a generation of magnetic components for 54V/48V to 12V converters. The effort specifically targets applications in the artificial intelligence (AI) and data center power conversion sectors. The collaboration's latest initiative involves 48V onboard power delivery solutions. The solutions – called Renesas P/N RAA228006/RAA226054 and ITG P/N SLA694719C-2R2MHF by the two companies – can deliver 1,000 W per phase. Compared to conventional 750W transformers, ITG's enhanced version provides a 46% reduction in transformer DC resistance (DCR), resulting in substantially reduced overall power loss.

www.itg-electronics.com

APEC 2024 Plenary Session Features Renowned Industry Experts

The annual Applied Power Electronics Conference, running February 25-29 at the Long Beach California Convention Center, will mark its 2024 event with an opening Plenary Session on Monday afternoon, February 26. The four-hour session will consist of six presentations delivered by visionaries representing industry and academia addressing topics of interest and concern to engineers engaged in applied power electronics technology. As always the APEC 2024 will address issues of immediate and long-term interest to the practicing power electronics engineer. Onsite at APEC 2024, day-long childcare for children of attendees will be available during the conference and exhibition from 8:00 a.m. to 5:00 p.m., from Tuesday to Thursday (Feb. 27-29).

www.apec-conf.org

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High Voltage IGBT, Hybrid & SiC MOS

High density • Low loss • High cycling

Efficient • Effective • Enabled

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Test & Measurement Solutions at APEC

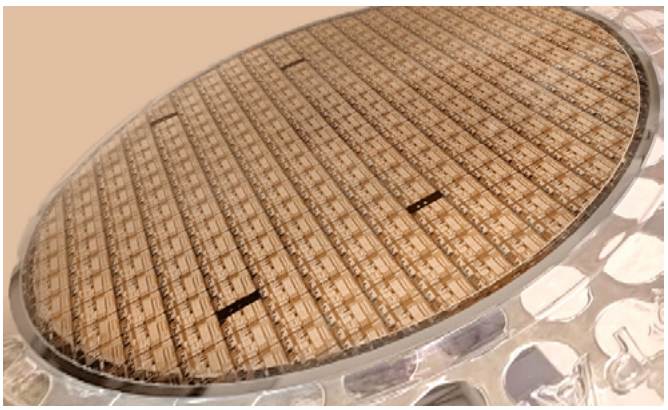
When APEC 2024 will open its gates in Long Beach, California on February 25-29, 2024, professional power test solution provider ITECH Electronics will show their power electronics testing instruments and solutions. This means that ITECH will exhibit all their series of T&M instrument products. For example, the ITECH upgraded AC source products such as IT7800, IT7900 and IT7900P help engineers to challenge MW level tests. The star product surely is the IT6000C Bi-directional DC power supply, which adopts the third generation SiC-base technology and integrates the source and sink function in one unit. Another product exhibited is the IT-M series, featuring "compact structure" and "high power density", which give users a wide range of choices to meet the diverse testing demands. The IT2800 SMU, winner of three T&M awards in 2023, complements this line-up.

www.itechate.com

CMOS-Compatible 200mm Process Technology

CEA-Leti has developed a 200mm gallium nitride/silicon (GaN/Si) process technology compatible with CMOS cleanrooms that preserves the high performance of the semiconductor material and costs less than existing GaN/SiC technology. In one of nine presentations at IEDM 2023, the institute said that current GaN high-electron-mobility-transistor (HEMT) technologies used in telecom or radar applications come on small GaN/SiC substrates and require processing in dedicated cleanrooms. The SiC substrates used to grow GaN layers are very expensive and available only in relatively small size. This R&D project developed GaN/silicon technology (GaN/Si) on 200mm and later for 300mm wafer diameters in CMOS-compatible cleanrooms to reduce substrate cost and benefit from existing high-performance cleanroom facilities. As a result, CEA-Leti's GaN/Si technology performance at 28 GHz is gaining ground on GaN/SiC technology in terms of power density.

"Our goal was to reach existing state-of-the-art GaN HEMT performance at ~30 GHz with a 200mm CMOS- compatible GaN/Si technology and to compete with GaN/SiC technology," said Erwan Morvan, CEA-Leti scientist and lead author of the paper, "6.6W/mm 200mm CMOS Compatible AlN/GaN/Si MIS-HEMT with In-Situ SiN Gate Dielectric and Low Temperature Ohmic Contacts".



"This work demonstrates that CMOS-compatible 200mm SiN/AlN/GaN MIS-HEMT on silicon technology is a promising candidate for applications like 5G/6G infrastructure, satcom, radar for UAV detection or earth observation. It should enable less expensive devices while keeping high power density, high efficiency, light weight and compactness," he said.

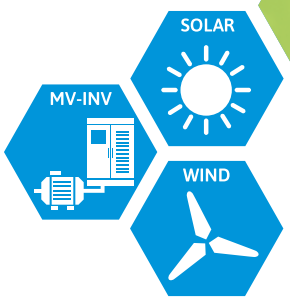
www.leti-cea.com

Opening Ceremony and Investor Day at Torrance HQ

Navitas Semiconductor held an Opening Ceremony and 2023 Investor Day at its new headquarters in Torrance, CA last December. Torrance Mayor, George Chen, and Dustin McDonald from the Office of the Governor of California joined Navitas' CEO and co-founder Gene Sheridan to speak and cut the ribbon, officially opening Navitas' headquarters. Around 100 Navitas staff are employed in Torrance for all aspects of GaN and SiC design, applications, test, characterization and quality plus finance, marketing and HR. Further team growth is planned for 2024, including a $20M investment to add SiC epi-growth capability for strategic manufacturing expansion.

At the event e. g. Dan Kinzer, co-founder and COO/CTO then introduced technology platforms including Gen-4 GaNSense half-bridges for motor drive and mobile fast chargers, GaNSafe – a protected GaN powertrain, GaNSense Control, and a bi-directional GaN power IC platform with up to 9x smaller chip size than legacy silicon MOSFETs or IGBTs. Sid Sundaresan, SVP for the GeneSiC product line added more detail on the Gen-3 Fast SiC platform.

www.navitassemi.com



PrimePACK™ 7G IGBT Modules

Upgrading to 1200 A in PP2, 2400 A/1200 V & 2400 A/1700 V in PP3+ with RC-Technology

FEATURES

- Newly developed 7G IGBT & FWD
- Improved solder material for higher reliability
- Higher lifetime at same ΔTj
- Increased output power
- Higher power cycling capability
- Lower conducting and switching losses
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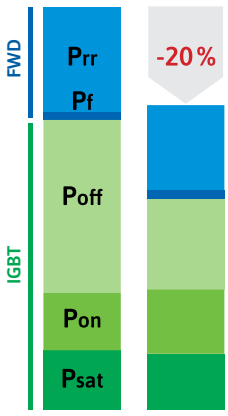

www.fujielectric-europe.com
www.americas.fujielectric.com/us-semiconductors

Fuji Electric
Innovating Energy Technology

Supplier Agreement for Silicon Carbide (SiC) Wafers

Infineon Technologies has formalized an agreement with silicon carbide (SiC) supplier SK Siltron CSS.

Under the agreement, SK Siltron CSS will provide Infineon with competitive and high-quality 150-millimeter SiC wafers, supporting the production of SiC semiconductors. In a subsequent phase, SK Siltron CSS will play an important role in assisting Infineon's transition to a 200-millimeter wafer diameter.

"For Infineon, supply chain resiliency is about implementing a multi-supplier strategy and thriving in times of adversity to create new growth opportunities and drive decarbonization," said Angelique van der Burg, Chief Procurement Officer at Infineon. "We are excited to partner with SK Siltron CSS to serve the growing SiC demand of our broad customer base with new energy-efficient and top-quality products, matching the highest standards in the SiC market."

"With decades of experience in silicon carbide materials and manufacturing, we bring unparalleled knowledge to our sustainably manufactured compound semiconductor solutions. This wealth of experience is a cornerstone in our partnership with Infineon," said Jianwei Dong, Ph.D., CEO of SK Siltron CSS. "This long-term supply agreement marks the synergy of our extensive expertise and Infineon's vision to make life easier, safer and greener for generations to come."

www.infineon.com

Financing Dedicated to Environmental Initiatives

Mitsubishi Electric Corporation announced that it has set the terms and conditions for issuing its first corporate green bonds in the Japanese market, as initially announced in a news release on November 10. The proceeds from the bonds will be used to construct a silicon-carbide (SiC) power semiconductor plant and upgrade related facilities.

Mitsubishi Electric has positioned sustainability as a cornerstone of its overall business, including initiatives to address climate change and other pressing issues facing modern society. This commitment to sustainability is reflected in the company's Environmental Sustainability Vision 2050 and Environmental Declaration to "protect the air, land, and water with our hearts and technologies to sustain a better future for all." Mitsubishi Electric has set a goal to aim for net zero greenhouse gas emissions from factories and offices by FY2031 and net-zero greenhouse gas emissions in its entire value chain by FY2051, and is striving to create and expand businesses that contribute to carbon neutrality.

In light of the company's active sustainability initiatives, 41 investors have announced their intention to invest in Mitsubishi Electric's first green bonds. Going forward, Mitsubishi Electric expects to accelerate efforts to contribute to the achievement of sustainable development goals (SDGs) in society for greater sustainability.

Environmental Sustainability Vision 2050

www.mitsubishielectric.com

STMicroelectronics Announces new Organization

STMicroelectronics moves from three to two product groups, AMPS and MDRF. The Analog, Power & Discrete, MEMS and Sensors Group (APMS) will be led by Marco Cassis, ST President and member of the Executive Committee, and the Microcontrollers, Digital ICs and RF products group (MDRF) will be led by Remi El-Ouazzane, ST President and member of the Executive Committee. The APMS Product Group will include all ST analog products, including Smart Power solutions for automotive as well as all ST Power & Discrete product lines including Silicon Carbide products complemented by MEMS and Sensors. APMS will include two Reportable Segments: Analog products, MEMS and Sensors (AM&S); Power and discrete products (P&D).

The MDRF Product Group will include all ST digital ICs and microcontrollers, including automotive microcontrollers but also RF, ADAS, Infotainment ICs. MDRF will include two Reportable Segments: Microcontrollers (MCU) as well as Digital ICs and RF Products (D&RF). Concurrent with this new organization Marco Monti, ST President of the former Automotive and Discrete Product Group, will leave the company. To complement the existing Sales & Marketing organization, a new application marketing organization by end market will be implemented across all ST Regions. This will provide ST customers with end-to-end system solutions based on the company's product and technology portfolio. The application marketing organization will cover the following four end markets: Automotive / Industrial Power and Energy / Industrial Automation, IoT and AI / Personal Electronics, Communication Equipment and Computer Peripherals. The current regional Sales & Marketing organization remains unchanged.

www.st.com

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HIOKI

Your **power inverter's efficiency** is more than **100 %?**

If your **power inverter measurements** show an efficiency of more than 100 % or if the measured values simply sound too good to be true then the reason is very likely a **measurement error caused by phase shift.**

Every current sensor produces a gradually increasing phase error in the high-frequency region which can make precise measurements on SiC & GaN based applications quite difficult.

HIOKI products can compensate this phase error because we make both **power analyzers** as well as the **specially designed current sensors.** This ensures that your power measurements at high currents and high frequencies are as **precise as you can expect them to be.**

Check our website to find out more about **phase error compensation** with **HIOKI power analyzers** and **current sensors.** Or simply contact us:

hioki@hioki.eu
www.hioki.eu

HIOKI EUROPE GmbH | Helfmann-Park 2 | 65760 Eschborn, Germany

Isolated Gate Driver Portfolio with Bipolar-Output Power-Thru IC

Adds Critical Safety Features to Help Protect Against High Operating Temperatures in Electric Powertrain Systems

Allegro MicroSystems announced the launch of the second product in its High Voltage Power portfolio. Allegro's AHV85111 isolated gate-driver IC adds critical safety features while simplifying the design of high-power energy conversion systems for e-Mobility and clean energy applications, including OBC/DCDC, solar inverter and datacenter power supply.

"Allegro continues to build upon the technology from our acquisitions in order to expand our High Voltage Power portfolio aimed at helping designers achieve their efficiency and power density needs in clean energy and e-Mobility systems," said Vijay Mangtani, Vice President and General Manager for High Voltage Power at Allegro. "The bipolar-output of our latest device improves noise immunity and significantly simplifies high-frequency power-converter designs."

Building upon Allegro's existing power-thru technology, the AHV85111 was designed to meet designer demands for a simple, streamlined and safe solution. The AHV85111 gate driver adds bipolar-output, a critical feature that significantly improves time to market by eliminating the need to design a complicated negative isolated DC power supply and removing unnecessary external components. Allegro's newest power-thru solution also adds crucial safety features that were designed to protect against high operating temperatures in electric powertrain systems, as well as reactions to noisy environments that may be present in microinverters in solar applications, power supply in datacenter applications or on-board chargers for electric vehicles.

The AHV85111 gate driver packs all the benefits of Allegro's power-thru technology, including 10x lower common-mode capacitance, a 50% smaller footprint, 10x noise reduction and a 50% efficiency improvement compared to competitor offerings, while also providing overtemperature protection that further improves the robustness of system.

www.allegromicro.com

Erik Rehmann, GVA expert for Quality Management

gva-power.de

„WHERE INNOVATION GOES IN SERIES: GVA"

Our Development, Production and Quality departments are separated by one floor and two flights of stairs – nothing else. Because all GVA experts share the same systemic understanding and the latest know-how. That´s why we are able to mass-produce innovative developments in the shortest possible time. With guaranteed quality – and gladly also for you!

Your GVA expert:
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GVA
POWER ELECTRONICS EXPERTS

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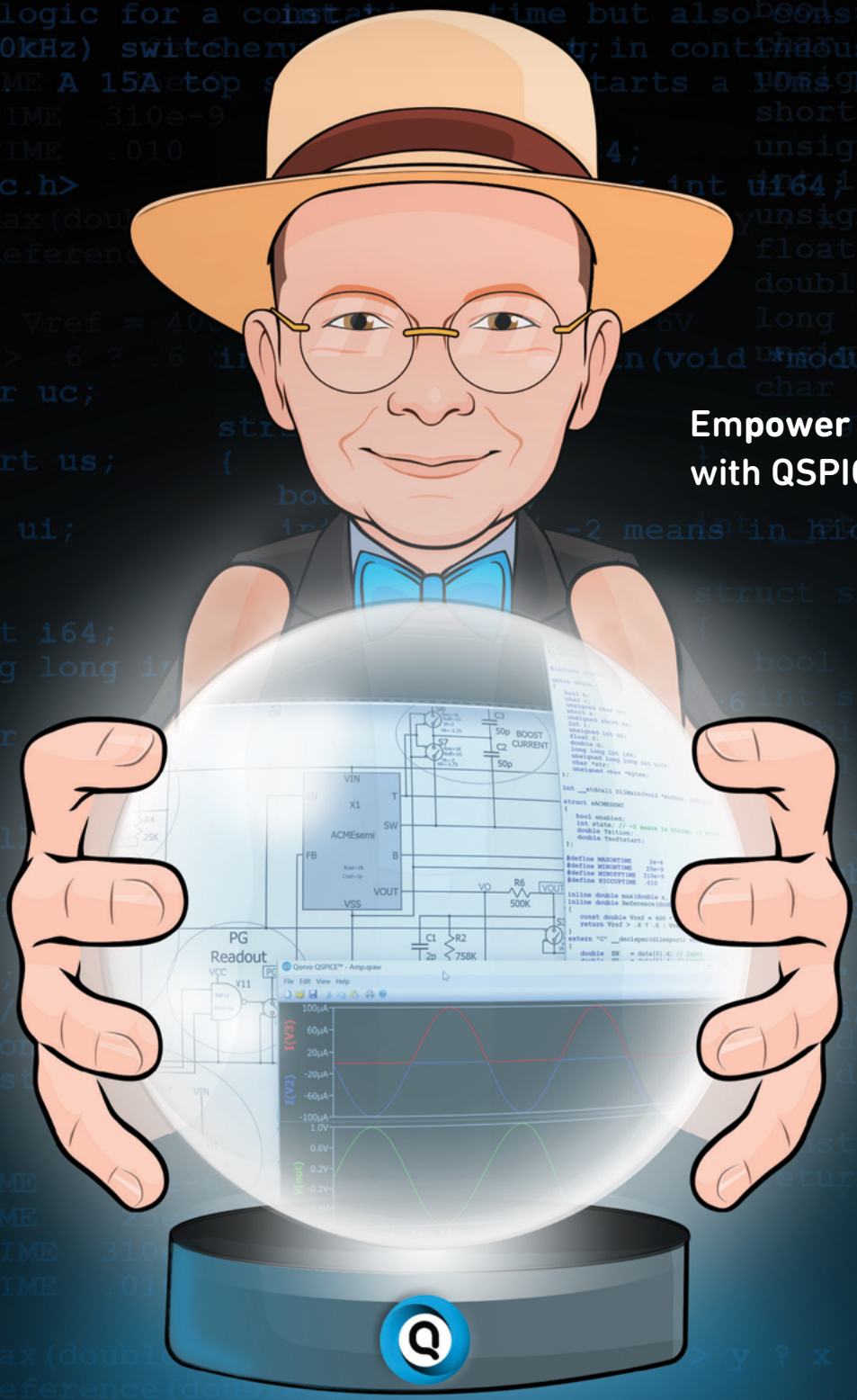

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Opening up the Electrification Market with TMR-Based ICSs

LEM recently announced a collaboration with TDK on next-generation tunnel magneto-resistance based integrated current sensors for electrification applications. The move recognizes the rapid growth in demand for current sensing technologies which in turn requires high volumes and cost-effective products. We caught up with Thomas Hargé, Vice President Global Product Management at LEM, to ask him about shifting industry trends and how this partnership with TDK might add value to customers.

By Bodo Arlt, Founder, Bodo's Power Systems

Bodo: How has the current electrification trend impacted the current sensing market and technologies?

Thomas Hargé

Thomas: Global decarbonisation is a major factor, with countries around the world embarking on what is nothing less than an electrification revolution. We are heading inexorably towards having an electrified planet and this is having an impact on a wide range of markets.

Of course, one of the biggest areas in all of this is the electrification of passenger vehicles. Transportation has been a massive contributor to excessive CO_2 emissions and the automotive sector is predicted to represent half of the entire current sensor market within the next five years. That's a game changer in terms of the technological advances that are needing to be developed within a very small timeframe.

How has LEM adapted its products or strategies to align with the electrification trend?

Since the very beginning of power electronics, LEM has been developing current sensing technologies for the rail, automotive and industrial sectors. The company has always worked very closely with customers and within key markets, optimizing existing technologies and co-designing solutions in conjunction with end users.

For at least the past decade, LEM has developed application-specific current sensors for electric vehicles (EVs) and hybrid electric vehicles (HEVs). As the market has accelerated, LEM has focused on working with customers to improve the integration of these sensors within inverters, on-board chargers (OBCs) – which convert AC to DC to charge a vehicle's battery pack – and battery management systems (BMSs).

Can you elaborate on the different technical requirements for current sensing in various applications and what trends are emerging?

Size is always a factor due to the limited space within an electric vehicle. Also, all components need to be of minimal size to make a vehicle as light as possible to minimise energy usage and extend the distances cars can drive between charges.

Improved integration within customer systems can often lead to breakthrough semiconductor solutions. That's why, since 2017, LEM has invested substantially in semiconductor development capabilities to develop integrated current sensors (ICSs). These are essentially a 'current sensor on a chip' and they enable users to build smaller systems.

Smaller power conversion systems can also be developed by using silicon carbide (SiC) or gallium nitride (GaN). These new transistors can switch faster and allow users to reduce the size of the magnetic components (ie chokes). As a consequence, current sensors need to be much faster and smarter than previously required while making it possible to measure higher frequency currents.

Again, integration is the key to compact designs, so the current sensing function is getting smaller and smaller. There is also more and more integration of software to simplify operation, provide additional features and minimise the amount of hardware in an EV.

Last but not least, but of equal importance, is the fact that several automotive applications require a 'safe' current measurement. That's why LEM has developed ISO26262 compliant sensors with safety levels that include quality management (QM) and Automotive Safety Integrity Level (ASIL) C.

How does LEM stay ahead in meeting the evolving technical demands across different applications?

Working with key customers and co-developing innovative solutions is vital to staying ahead in the market and being able to satisfy demand. As touched on earlier, LEM's investment in semiconductor technology has enabled the company to accelerate the miniaturisation of its sensors.

By LEM investing in new sensing technologies such as tunnel magneto-resistance (TMR) through its collaboration with TDK, the company is able to develop faster, more accurate and lower power sensors. At the same time, LEM has made significant investments in software capabilities so as to make the systems it develops smarter than their predecessors. Examples of such investment include a purpose-built R&D centre in Lyon, France, and setting up a dedicated team in Bulgaria.

How does LEM assess today's landscape in the current sensing market?

Over recent years, LEM has observed how the growth in the automotive market through increased electrification has attracted several companies from the semiconductor industry who are expanding their input in the sector. There has also been some growth in the number of classical automotive tier 2 producers (ie component manufacturers who supply the OEM automakers) providing some solutions.

What strategies does LEM employ to stay competitive and adapt to changing market dynamics?

In addition to the efforts on the technology side described above, LEM is the only player in the sector that focuses solely on current sensors. That has resulted in the company today having the broadest portfolio of current sensors, which means it has been able to pick the right technology for every new challenge. TMR is another technology that will expand this portfolio of solutions. Furthermore, LEM has accumulated a tremendous level of know-how in the area of current measurement. This has played a key role in en-

abling LEM's engineers to develop accurate and reliable sensors in customers' applications.

How does LEM position integrated current sensors (ICSs) as a solution to the challenges of 'smaller, smarter, cheaper' devices?

LEM considers ICSs to be the natural evolution for current sensors. In fact, integrated sensors are actually just smaller versions of their predecessors. Something that is often not understood is that all the challenges that are involved in measuring current are amplified through miniaturisation. This means it is absolutely critical for players operating in this sector to have a deep understanding and experience on critical parameters such as di/dt, dV/dt and partial discharges to name a few.

Can you provide examples of how ICS technology addresses specific challenges in the market?

One of the biggest attributes of ICSs is their size. For example, a typical application where a traditional LEM sensor would be too big would be in electric bikes. Thanks to ICS technology, 8-SOIC (3.90mm wide) sensors such as GO 20 SME Hall effect current transducers are now small enough to fit into an e-bike motor while delivering precise torque control. The extremely low profile sensors feature galvanic separation between the primary and secondary circuits, insulated test voltage of 2500V RMS and low power consumption. They also have high immunity to external interference, superior insulation capability, no magnetic hysteresis and low electrical resistance (0.9 mΩ).

Within its integrated circuit sensor range, how does LEM's use of TMR technology specifically address application challenges?

Most ICSs today use Hall elements to sense the magnetic field generated by the current to be measured. After spending many years improving Hall sensors, LEM had reached a point where making one parameter better (such as speed) meant compromising on others (including accuracy and power consumption). The beauty of TMR is that it delivers all three – better speed and accuracy and lower power consumption all at the same time. The compromises have been removed and that will go a long way towards being able to meet the challenges of specific applications.

What applications benefit the most from TMR technology, and why?

On-board chargers in EVs will be the first application to benefit from TMR technology because they require very fast current measurement. Second in line will be solar inverters, with integrated current sensors providing an excellent offset drift over temperature (which is essential on the AC side).

How does the partnership with TDK enhance LEM's ability to deliver solutions to the market?

TDK has developed over time a very deep know-how in TMR technology. The combination of the company's TMR knowledge and LEM's experience in ICS development will make it possible to set a new standard in ICS performance for OBCs, solar inverters and other applications such as autonomous mobility. LEM selected TDK as a partner based on its best-in-class technology performance as well as reliable supply, automotive quality and process maturity. The collaboration has been created to produce a TMR-based sensor that is faster, more accurate and with lower noise than existing solutions.

How does the collaboration with TDK contribute to time-to-market and the reliability/quality of LEM's solutions?

It takes many years to develop a good TMR and a top quality ICS. By joining forces, the two companies will use their existing technologies to shorten significantly the time it would have taken for either of them to bring a top-class, game-changing product to the market. TDK develops TMR dies for LEM who incorporates them into integrated current sensors for the sectors mentioned earlier. The current sensor market requires high volumes and cost-effective products and this collaboration will definitely deliver those.

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Controller HIL Testing for GaN and SiC Converters

The high switching frequencies of converters with GaN and SiC components pose a challenge for real-time simulators used for hardware-in-the-loop testing of control systems. When the switching frequency of power semiconductors exceeds 100 kHz, it is not sufficient to reduce the simulation step to just below one microsecond. In addition, the gate signals need to be oversampled and averaged over one simulation step. This approach works well on CPU- and FPGA-based simulators for hard-switching inverters in continuous conduction mode. However, it becomes inaccurate for resonant converters or dual active bridges, where the currents frequently change direction or enter discontinuous conduction mode. For the accurate simulation of such converter topologies, very small simulation steps of a few nanoseconds are required, which can only be realized with special algorithms on an FPGA.

By Jost Allmeling and Bryan Lieblick, Plexim

Electrical circuit simulation helps design engineers predict and analyze the behavior of an electrical device or system before a prototype is built. Simulation allows engineers to create a model or virtual prototype for the device, and perform tests under normal and faulty operating conditions. Since modifications to the model can be made quickly, simulation accelerates the development process and reduces time-to-market for new products. Simulation is not only helpful in an early design phase, but also for testing the correct operation of an existing device that will be part of a larger system.

In power electronics, digital real-time simulators are increasingly employed to test and validate control equipment without the actual power circuit being available. The actual power circuit, which represents the controlled system, is replaced by an appropriate dynamic model computed on the simulator. Since the control equipment is embodied as electronic hardware, this use case is referred to as controller hardware-in-the-loop (HIL) testing. HIL simulations allow testing both the control hardware and software in a safe environment.

When simulating power electronics in real time, the small time constants and fast dynamics of the electrical circuit pose challenges. To make the control equipment under test operate in the same way as when it is connected to a real power circuit, the real-time simulator must feature both high fidelity and low loop-back latency. This means, the simulation results must accurately represent the real voltages and currents in the electric circuit, and they need to be computed and output within few microseconds after a signal has changed at the simulator's input.

With the advent of wide bandgap devices such as GaN and SiC MOSFETs, the switching frequencies of power converters have advanced into the MHz range. This is a particular challenge for real-time simulators, as their minimum simulation time step typically lies between 100 ns and a few microseconds. However, in order to capture a PWM signal with sufficient accuracy, it must be sampled with a rate of at least 100 times the switching frequency. In the case of a switching frequency of 1 MHz, this translates into a sampling interval of 10 ns or less.

Two techniques that facilitate real-time simulations with such small sampling intervals are sub-cycle averaging and Nanostep™. While sub-cycle averaging can be applied to a wide class of inverters primarily operating in continuous conduction mode (CCM), a Nanostep solver is perfectly suited for the simulation of high-frequency and resonant DC/DC converter topologies such as the dual-active bridge (DAB) and LLC.

Common power supply architectures combine an AC/DC converter and a high-frequency DC/DC converter. A typical example is an EV charger consisting of a 3-phase active front-end (AFE) and a DAB as shown in Figure 1. In this 10 kW charger, which is based on wide bandgap technology, the AFE operates in CCM at 140 kHz while the DAB switches at 500 kHz.

With upcoming firmware upgrades for the RT Box 2 and 3, such a charger circuit can be simulated in its entirety on the FPGA fabric inside the RT Box. The AFE would be simulated with sub-cycle averaging, while the DAB would require a dedicated Nanostep solver. This combination of solver techniques enables highly accurate real-time simulations of power converters with high switching frequencies.

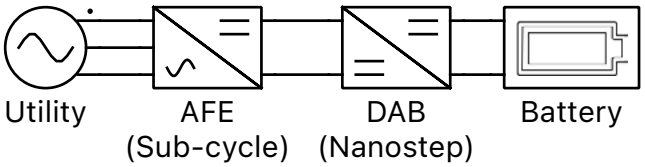

Figure 1: System schematic for EV charger with active front-end (AFE) and dual-active bridge (DAB).

Sub-cycle averaging

In power electronic applications, many inverter-converter systems such as buck converters, boost converters, diode rectifiers and voltages source inverters (VSIs) can be realized with one or more half-bridges. These half-bridges consist of series-connected power semiconductors, each of which can be naturally commutated devices (e.g. diodes), forced commutated devices (e.g. IGBTs) or a combination of both.

In most applications, the half-bridges are connected on the DC side to a capacitor or voltage source. Under normal operation it can be assumed that the DC voltage v_{dc} is positively biased, since otherwise the diodes would short circuit the DC link. During operation, the phase terminal is either switched to the positive or negative DC link voltage or remains unconnected.

For sub-cycle averaging, such half-bridges are modeled with a combination of two series connected diodes and multiple controlled voltage and current sources in order to increase the fidelity of real-time simulations. This modeling approach is illustrated in Figure 2 for a VSI half-bridge. The voltage sources v_{a1} and v_{a2} are controlled by the switching signals s_p and s_n. They apply the DC voltage v_{dc} to the phase side. Likewise, the current source i_{dc} is controlled by the

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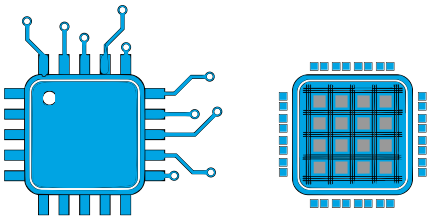

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same switching signals applying the phase current i_{a1} or i_{a2} to the DC side.

The two diodes are required to simulate natural commutation and discontinuous conduction mode (DCM). Depending on the direction of the phase current, the lower or upper diode will conduct which applies the corresponding phase voltage and DC current. If none of the diodes conduct, the half-bridge has entered DCM, which means i_a is zero.

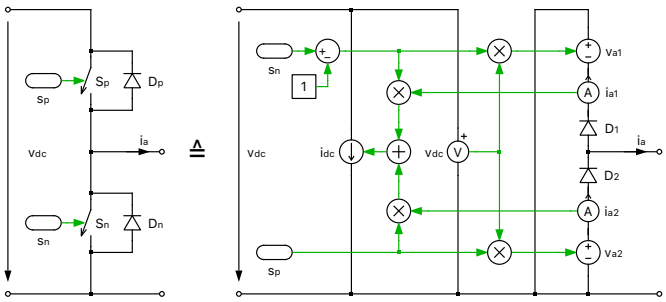

Figure 2: Sub-cycle average model for a VSI half-bridge.

The key advantage of sub-cycle averaging is that the switching signals can not only be binary signals representing the on-state (s = 1) and off-state (s = 0) of the device, but can also be short-term average values ($0 \le s \le 1$) representing the relative on-time or duty cycle of the device during a simulation step. These average values can be obtained by sampling the PWM signals at each FPGA clock cycle, which is typically shorter than 10 ns. Even with high switching frequencies and simulation steps two orders of magnitude larger than the FPGA clock cycle, the resulting phase current is essentially accurate because the applied volt-seconds of the average signals correspond to the volt-seconds of the original PWM signals. With large simulation steps, however, not all switching harmonics can be preserved. If the step size is too large there may be a gross error in the calculated voltages and currents.

The main disadvantage of sub-cycle averaging is the inaccuracy caused by the zero crossing of the phase current. As the direction of the phase current is determined only once per simulation step, slightly incorrect volt-seconds may be applied during the step in which the current has crossed zero or has entered DCM. While this inaccuracy is acceptable for inverters operating in CCM and without frequent changes in the current direction, such as grid-connected VSIs, this may not be the case for other converters, especially naturally commutated converters, operating at high switching frequencies.

Figure 3 depicts the 3-phase AFE circuit from the EV charger example. The AFE with SiC MOSFETs switching at 140 kHz serves as the benchmark model for validating the sub-cycle averaging technique. In this circuit model, the load of the DAB stage is represented by an equivalent resistor R_{out}.

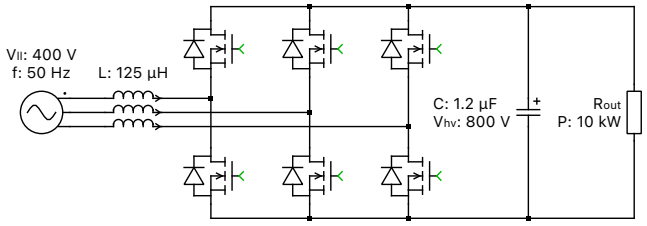

Figure 3: AFE circuit with SiC MOSFETs.

Figure 4 shows the input currents of the AFE during a step change from half load to full load. The reference results were generated by offline simulations in PLECS with a variable step solver and ideal switches. They are compared with the waveforms obtained from real-time simulations with the RT Box. The model step of 400 ns corresponds to the step size that can be achieved on an RT Box 2 or 3 by using the new FPGA-based circuit solver with sub-cycle averaging. The control signals for the MOSFETs are generated by an open-loop controller to allow a direct comparison between the two different modeling approaches.

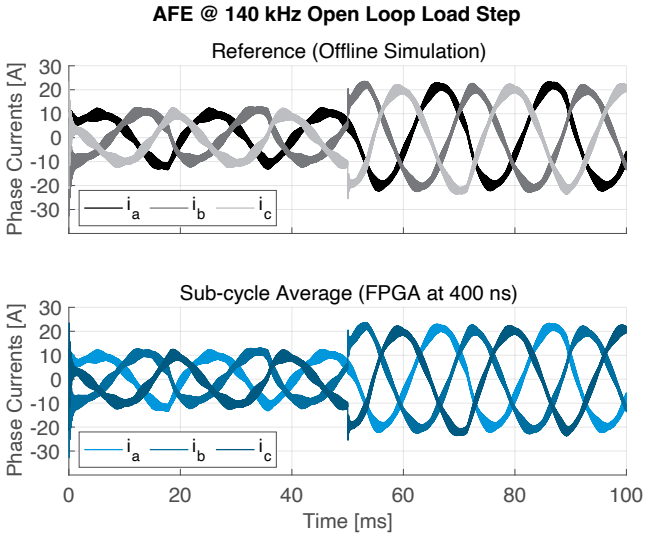

Figure 4: Offline simulation with PLECS compared to real-time simulation on the RT Box.

The comparison of the phase currents demonstrates the accuracy of the sub-cycle average model. Figure 5 shows the AC current in phase A for a single cycle of line frequency. The FPGA-based simulation at 400 ns closely matches the reference waveform. However, the sub-cycle average approach requires a sufficiently small model step size for an accurate solution. At a step size of 2 µs, which is representative for computing the sub-cycle average model on a CPU core of the RT Box, the current waveforms exhibit a large error.

This error is caused by the delayed detection of changes in the current direction, which can occur when the PWM pulses are shorter than the step size of the simulation. In the model in Figure 2, the peak values of the averaged voltages v_{a1} and v_{a2} may not be large enough to make the phase current commutate directly from one diode (D_1 and D_2) to the other. Instead, both diodes may open and clamp the current to zero. This effect can be observed in Figure 5, where at a step size of 2 µs the phase A current is distorted around the zero crossings. The same behavior in phases B and C manifests itself in distortions near the peak of the phase A waveform via a shift in the neutral voltage.

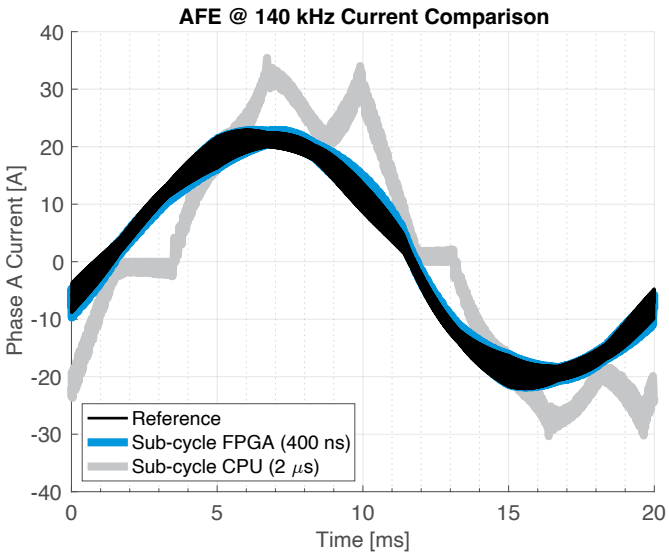

Figure 5: Phase A current waveform over one line cycle.

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Figure 6 illustrates in detail how the direction of the phase current changes from negative to positive. Despite the repeated zero-crossings, the FPGA-based simulation deviates only slightly from the reference. With the 400 ns step size, the solver executes nearly 18 times within a switching cycle, so the averaged voltage values are often close to the instantaneous voltages. Occasional clamping of the current to zero, caused by open diodes, is transitional and has only a minor impact on the results. On the contrary, if the voltages are averaged over a CPU model step of 2 µs, they fail to commutate the current.

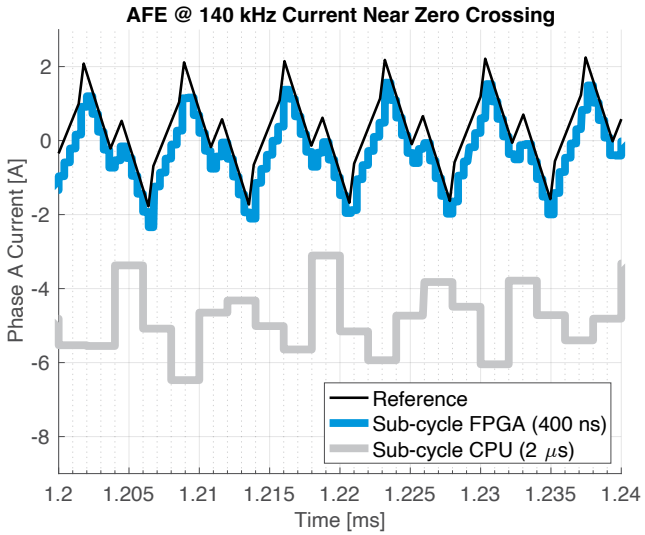

Figure 6: Detailed view of phase A current waveform.

Nanostep™

As discussed earlier, the sub-cycle average approach becomes inaccurate for power electronic converters where the direction of the phase current changes frequently. This is especially true for DC/DC converters with an inductive AC link, where the power transfer is very sensitive to the phase shift between the current and the PWM signals. A delayed zero crossing detection of the AC current can lead to considerable errors. This is because positive, negative and zero current each correspond to a different circuit topology, which is governed by another set of differential equations.

In order to detect zero crossings as fast as possible, Plexim has developed the Nanostep solver that will be available for the RT Box later this year. In a Nanostep simulation, the values for the inductorcurrents and the voltages of the resonant capacitors are updated with each FPGA clock cycle. Since the calculation of a new value requires a pipeline of arithmetic operations and takes multiple clock cycles, the values for all possible topologies are computed in parallel. The validity of a topology depends on the most recent gate signals and the latest direction of the inductor current. An inductor current that changes direction or is clamped to zero represents a boundary condition that limits the validity range of certain topologies. The decision which topology must be applied is only made after all values have been calculated and is based on the boundary conditions at that point in time.

A Nanostep model of the EV charger's DAB stage is shown in Figure 7. The converter switching frequency is 500 kHz with a dead time of 120 ns. A phase shift between the primary and secondary switch modulation controls the power transfer.

The Nanostep solver incorporates the switching network and energy storage elements of the converter. Gate signal sampling, inductor current integration, and current zero-crossing detection all occur at the FPGA clock cycle of 5 nanoseconds or less. With a 5 ns sample rate, the Nanostep solver can detect phase shifts as low as 0.5 % for a 500 kHz switching frequency.

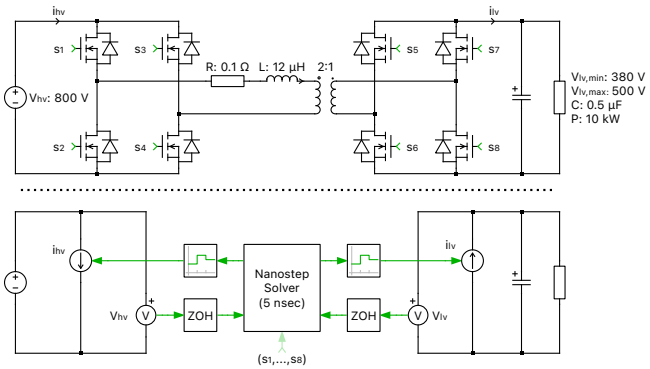

Figure 7: Nanostep model for a dual active bridge interfacing with an external circuit.

The external circuit dynamics of interest, namely the input and output capacitor voltages v_{HV} and v_{LV}, are usually significantly slower than the dynamics of the internal switching network. The external circuit is simulated using a generic solver implemented on the FPGA or CPU with a much larger model step. Typical step sizes range from a few hundred nanoseconds to a few microseconds. In this application, the 400 ns model step of the AFE is used as the communication interval with the Nanostep solver. The inputs to the Nanostep solver are the terminal voltages of the converter, sampled at the model step. The Nanostep solver averages the converter's input and output currents over one model step so that the currents i_{HV} and i_{LV} injected into the external network are correctly calculated.

The limitations of the Nanostep solver are due to the interface with the external circuit that is solved at a larger model step. The voltages at the converter terminals are assumed to be constant over a model step. The model step also dictates the update rate of the analog hardware output, which in turn affects the loop-back latency. Lastly, internal fault conditions are not simulated, but can be detected when any gate signals within the 5 ns sampling interval would result in shorting the DC terminals of the converter.

Figure 8 benchmarks the accuracy of the Nanostep solver against offline PLECS simulations with ideal switches and against a hypothetical sub-cycle average model with a 50 ns step size. Currently, the 50 ns model cannot be realized on the RT Box. The converter operates with a constant phase shift of $0.1T_{sw}$ or 200 ns. With the larger step size, averaging the gate signals over the 50 ns interval leads to an error in the output current. The zero crossings of the current during the dead time interval are also missed. Comparing

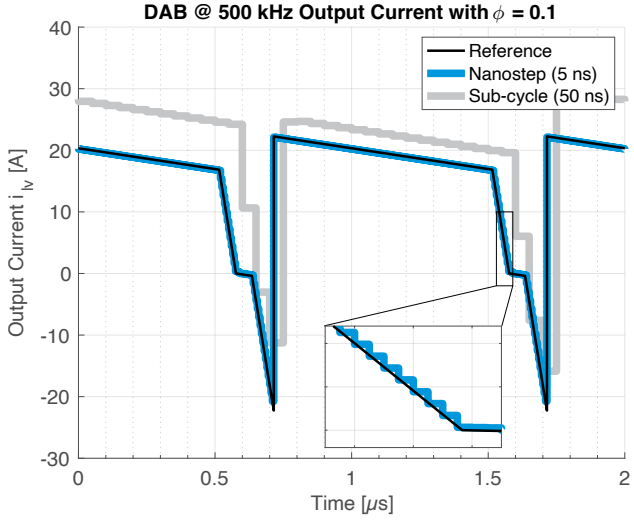

Figure 8: Output current of DAB simulated with 5 ns and 50 ns step size.

the average current over a model step, the Nanostep solver and reference solution are accurate to within 1% while the model with a 50 ns step size has an error of 40 %.

Using the average values of the 5 ns Nanostep solver calculations as the interface to the external circuit retains the large-signal dynamics of the converter's input and output ports. Figure 9 shows the model response for a step change in modulator phase with a constant resistive load. The converter starts at 500 V output at rated power, steps to a lower power level due to a decrease in phase shift, and then returns back to the initial phase. The voltage dynamics of the Nanostep solver in combination with a 400 ns model step closely match the reference solution. The additional phase lag is due to the current averaging of the Nanostep solver and the model step duration. The sub-cycle average model, though, is not usable as it delivers excess power and the output voltage therefore never reaches the expected steady-state output voltage.

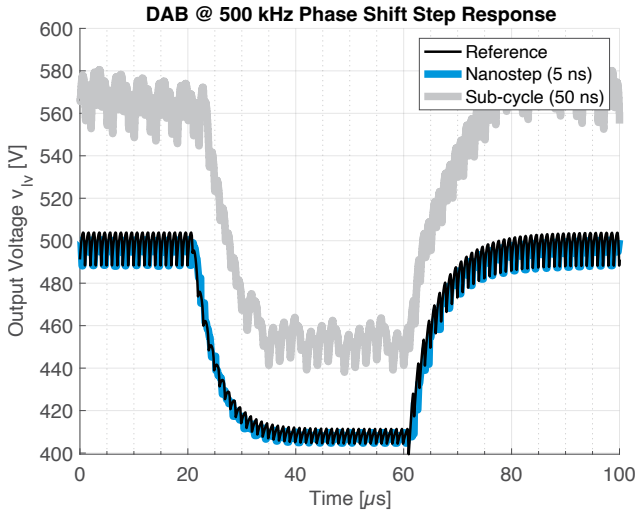

Figure 9: 500 kHz DAB response to a step change in modulator phase shift.

Conclusion

Real-time simulation can be used to test and validate the control equipment even for next-generation power converters based on SiC and GaN. Due to the high switching frequencies and short time constants of converters with wide bandgap devices, real-time simulators must capture the gate drive signals with sampling intervals of a few nanoseconds and use special numerical techniques to detect current zero crossings with high accuracy in time.

Plexim has developed powerful algorithms to meet these requirements: Sub-cycle averaging is a versatile method for simulating voltage source inverters operating mainly in CCM. In addition, the new Nanostep solver enables real-time simulation of high-frequency and resonant DC/DC converters operating well above 100 kHz. The Nanostep solver detects changes in current direction with a resolution of 5 ns, making it perfect for selected topologies where the current frequently changes direction or enters DCM.

Firmware upgrades free of charge, to be released in 2024, will enable the RT Box 2 and 3 to simulate sub-cycle average and Nanostep models on the integrated FPGA. Benchmark simulations of a 3-phase AFE at 140 kHz and a DAB at 500 kHz show that these real-time simulation techniques produce highly accurate results.

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Improved Application Efficiency with Novel MOSFET Technology

MOSFET technologies are excellent switches in a wide range of applications with varying requirements, including power management circuits and motor drives. The commercial introduction of vertical diffused MOSFET structures with a lateral channel offered an appealing alternative to bipolar technologies [1]. But the high on-state resistance limited the current-handling capabilities of these devices, and hence their use in power electronic applications.

By Ralf Siemieniec, Senior Principal Engineer, Simone Mazzer, System Engineer, Cesar Braz, Product Definition Engineer, and Elvir Kahrimanovic, Principal Engineer, Infineon Technologies

The appearance of the first trench gate MOSFETs marked a milestone for the broad adoption of field-effect transistors in power electronics [2]. Moving the channel vertically, the device virtually removed the JFET region and reduced the on-state resistance. Advancements in manufacturing technology increased the cell density and with it, the channel width, offering progressively lower on-state resistances. However, this cell density increase also brought significant disadvantages. The gate-drain and gate-source capacitance both increase linearly with the number of trenches, i.e., with the cell density.

A MOSFET is uniquely controlled through its gate terminal, so the gate driver circuitry must provide the total gate charge (Q_G) required to turn on the transistor. In the case of high switching frequency applications like SMPS, the lowest gate charge is desirable to proportionally reduce driving losses. Larger gate-drain charge (Q_{GD}) values impact the transient speed, resulting in increased switching losses, forcing longer dead-times.

The introduction of charge-compensated structures, exploiting the same principle as superjunction devices, marked the beginning of a new era. The first of these devices used an insulated deep field-plate as an extension of the gate to enable the lateral depletion of the drift region in the off state. This achieved a substantial reduction in the on-state resistance [3]. It was only by isolating the field plate from the gate and connecting it to the source that devices with improved gate and gate-drain charges were created [4]. When introduced, these devices showed best-in-class performance with the following features, eventually becoming an industry standard:

- Low gate charge and gate-drain charge characteristics
- High switching speeds
- Good avalanche ruggedness

New MOSFET devices should improve all figures of merit, as losses are associated with both charges (switching) and on-state resistance (conduction). A novel cell-design that explores a true three-dimensional charge compensation meets these requirements [5].

State-of-the-art power MOSFET technologies commonly use an insulated deep field-plate, separated from the gate electrode above, combined with a stripe layout (figure 1, left). The new approach separates the field plate trench (now forming a needle-like structure) from the gate (now forming a grid surrounding the needles, figure 1, right). This increases the silicon area for current conduction and reduces the overall on-state resistance.

To further reduce the $FOM_G = R_{DS(on)} \times Q_G$ and $FOM_{GD} = R_{DS(on)} \times Q_{GD}$ values, the gate trench is completely redesigned, minimizing its lateral extension. However, the reduced dimensions of the gate impose a challenge because using polysilicon as the gate material results in unacceptably large internal gate resistances. The standard approach to address this problem is to introduce gate fingers to shorten the gate element lengths, thus reducing the overall distributed gate resistance.

Unfortunately, these finger structures consume space at the cost of the active area available for current conduction. Introducing gate fingers will therefore reduce the internal gate resistance but increase the on-state resistance of the chip. To avoid this area wastage, a metal gate system is introduced to reduce the internal gate resistance and significantly improve the gate resistance uniformity over the chip.

Together with the direct connection of the field plates to the source metal, a new device setup is realized. This setup ensures a fast and homogeneous transition at turn-on and turn-off, minimizing switching losses and reducing the risk of an unwanted (dV/dt)-induced parasitic turn-on of the MOSFET. The direct connection of the field plates also practically eliminates any resistance in series with the output capacitance, minimizing the conduction losses during charging and discharging.

Figure 2 summarizes the impressive device parameter improvements for various voltage classes in all relevant parameters over the predecessor technology. Thanks to the new advanced cell design, the device on-state resistance is dramatically reduced, allowing a much higher current in the same package footprint. The innovative gate-trench engineering of the new device also greatly improves both gate- and gate-drain specific capacitances, reflected in the respective figures-of-merit: FOM_G and FOM_{GD}.

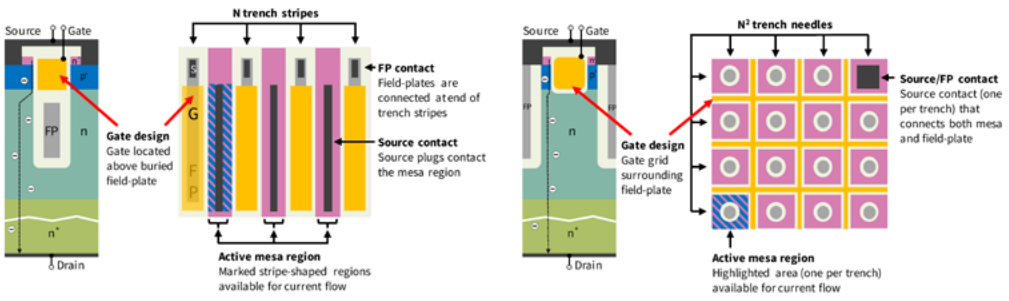

Figure 1: Comparing the typical trench MOSFET structure with an insulated field plate connected to source and the top view of the associated stripe layout (left) with the new MOSFET structure using a separated gate and the grid-like chip layout (right)

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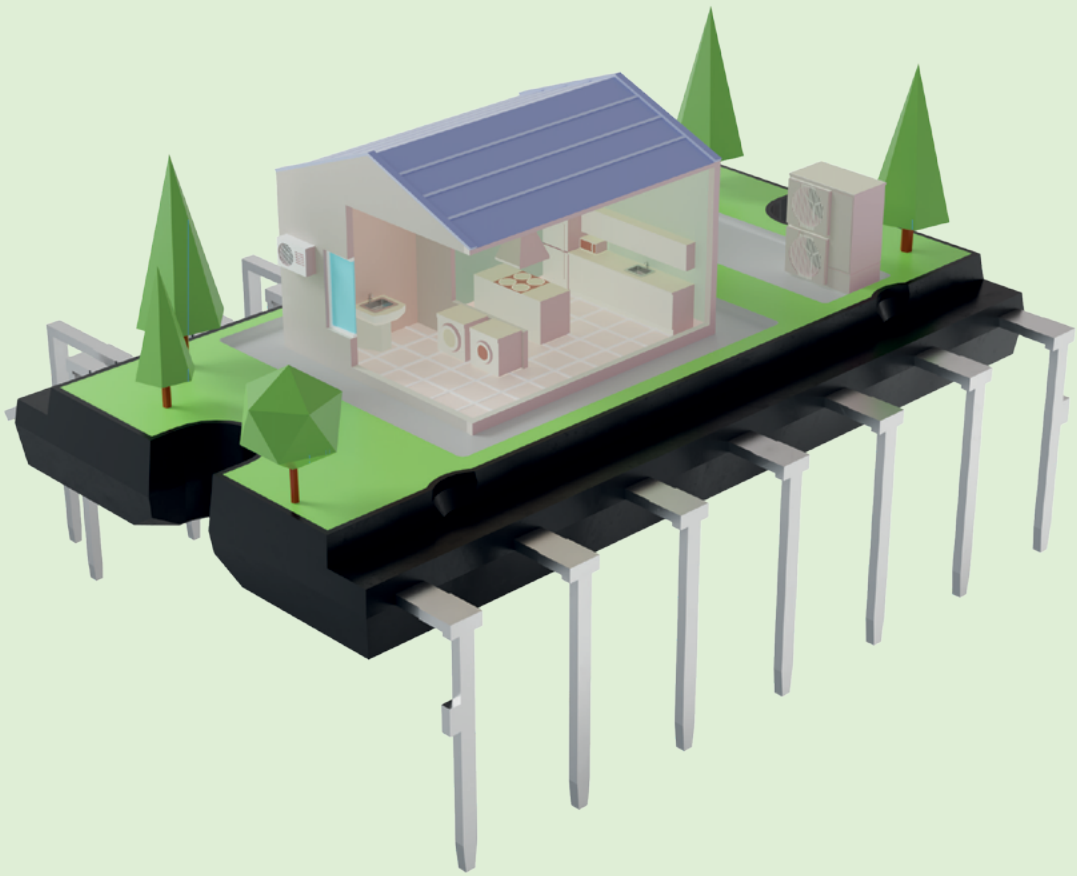

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Changes for the Better

FOM_G reduction helps achieve better efficiencies, especially at light load conditions because of reduced driving losses. This is particularly important for an SMPS operated at high switching frequencies and in applications like motor drives with a large number of paralleled MOSFETs. Here, the low gate charge also relaxes the requirements on the gate driver's current capability. Additionally, the low Q_{GD} enables fast switching transients, lowering switching losses.

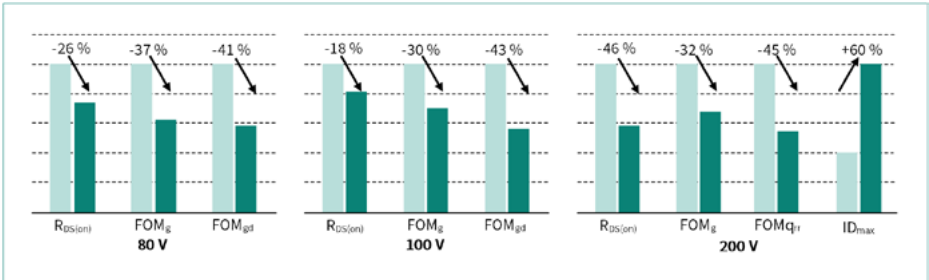

Figure 2: Improvement in key performance parameters for best-in-class 80 V, 100 V, and 200 V devices

In case of the new 200 V technology, it is additionally important to reduce the reverse recovery charge with respect to the predecessor technology generation. This is important for:

- Lowering the switching losses
- Improving the EMI behavior
- Ensuring a high commutation ruggedness

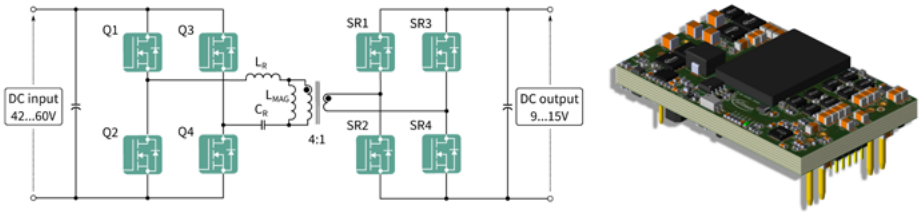

Figure 3: Schematic of the 1 kW 4:1 LLC IBC and 3D view of the board in a standard quarter-brick format

DC-DC converters are extensively utilized in telecom and datacom power systems, commonly as isolated DC-DC intermediate bus converters (IBC) in the overall conversion chain from a nominal 48 V input. These converters step down the line voltage to an intermediate voltage, such as 12 V, to feed the downstream point-of-load (PoL) converters. Because of continuous improvements in MOSFET technology, power density has increased enough for a regulated IBC in a standard quarter-brick form factor to deliver up to 1 kW of power continuously.

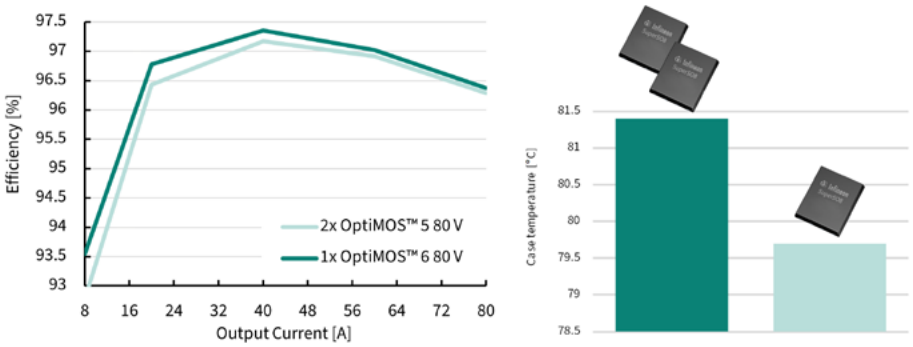

Figure 4: Comparison of the gained efficiency improvement and the device temperatures in the LLC IBC at V_{IN} = 54 V

In modern datacenters, the nominal 48 V distribution bus ranges between 40 V and 60 V. The resonant LLC topology (figure 3, left) is a popular choice for IBCs, enabling high-efficiency conversion with high power density [6]. Operating with a fixed switching frequency, the LLC IBC behaves like a DC transformer (DCX) realizing a fixed-ratio down conversion (e.g., 4:1). The LLC DCX converter attains zero-voltage switching (ZVS) in the primary-side switches Q1 to Q4 regardless of the output load level.

ZVS is achieved through the transformer magnetizing inductance L_{MAG}. Its value is defined accounting for the MOSFETs' output capacitance C_{OSS}, as the magnetizing current I_{LMAG} must fully charge and fully discharge C_{OSS} during the dead-time. This condition must be fulfilled over the entire input voltage range, ensuring all primary-side MOSFETs operate in soft switching. Each MOSFET in the full bridge is switched at a constant 50 percent (minus the dead-time) duty cycle ratio.

Parameter	Value
Transformer turns ratio	4:1
LLC converter resonant frequency	310 kHz
Primary-side full-bridge MOSFETs	ISC014N08NM6, 80 V, PQFN 5 mm × 6 mm, $R_{DS(on),max}$ = 1.45 mΩ
Secondary-side full-bridge MOSFETs	IQE006NE2LM5, 25 V, PQFN 3.3 mm × 3.3 mm Source-Down, $R_{DS(on),max}$ = 0.65 mΩ, two-paralleled

Table 1: 1 kW test board parameters with new technology primary-side MOSFETs

The inductor L_R forms a series-resonant circuit with the resonant capacitor C_R, building up a quasi-sinusoidal current fed through the transformer to the secondary side, rectified by the synchronous rectification stages SR1 to SR4. The SR MOSFETs operate in ZVS and zero-current switching (ZCS), virtually eliminating most losses associated with their commutation.

Figure 3 (right) shows the employed 1 kW test board with a standard quarter-brick form factor with the parameters detailed in table 1.

The significantly improved device parameters allow the replacement of two paralleled OptiMOS™ 5 BSC030N08NS5 power MOS-FETs in each position of the primary full bridge with one OptiMOS 6 ISC014N08NM6 power MOSFET. Figure 4 compares the efficiency and device temperatures. With the new devices, the overall ef-ficiency improves over the full output current range, with a peak improvement of almost 0.8 percent at low load. Despite using one device instead of two, the package temperature also decreases.

This efficiency improvement comes from the lower gate and gate-drain charges and the practically eliminated internal series resis-tance to the output capacitance. The LLC avoids losses because of the stored charge in the output capacitance of the MOSFET be-cause this charge swings from one MOSFET to the other instead of being dissipated during a hard turn-on of the device. However, this swing current causes conduction losses because of PCB tracks, transformer windings, and the internal equivalent series resistance connected to the MOSFET output capacitance, the latter being mas-sively reduced with the new devices.

Inverting buck-boost DC-DC converters in -48 V telecom power systems are used in the supply of the RF power amplifiers (RFPAs),

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which need supply voltages ranging from +28 V (for use in LDMOS RFPAs) up to +50 V (for use in GaN RFPAs).

The investigated evaluation board provides an output voltage of 12 V, suitable for telecom equipment, other than RFPA, which do not require functional/safety isolation. This configuration requires MOSFETs with a blocking voltage of 100 V, making it an excellent vehicle to study the performance of the new OptiMOS 6 100 V MOSFET in a soft-switching topology. The board, based on an interleaved (two-phase) inverting buck-boost, delivers up to 600 W from an input voltage range of -36 V to -60 V. Figure 5 shows the basic schematic and the resulting board.

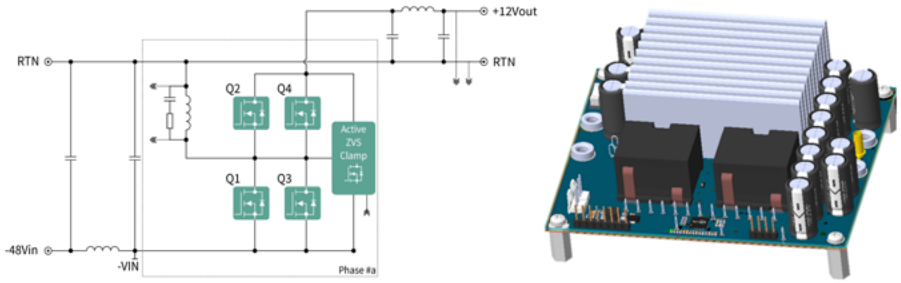

Figure 5: Basic schematic of one phase of the inverting buck-boost DC-DC converter and a view of the realized evaluation board

The design uses a novel active clamp auxiliary circuitry that transfers the reverse recovery charge Q_{RR} from the synchronous rectifier MOSFETs Q2 and Q4 towards the output in a non-dissipative way. This achieves ZVS turn-on for the control switches Q1 and Q3. The active clamp circuit drives down the overall switching losses in the unit, enabling the use of best-in-class devices with the lowest on-state resistance, and supporting a dramatic increase in power density [7].

Figure 6 compares the measured efficiencies between the predecessor OptiMOS 5 BSC027N10NS5 and the new OptiMOS 6 100 V ISC022N10NM6 MOSFETs. The results clearly illustrate the huge impact of this advanced technology with an impressive efficiency gain of up to 1 percent. The higher efficiency goes hand-in-hand with the lower losses of 7 W, indicating a power density increase of 15 percent. This loss reduction is due to the lower on-state resistance, lower gate charge, and lower reverse-recovery charge being transferred to the output by the active ZVS clamp circuit.

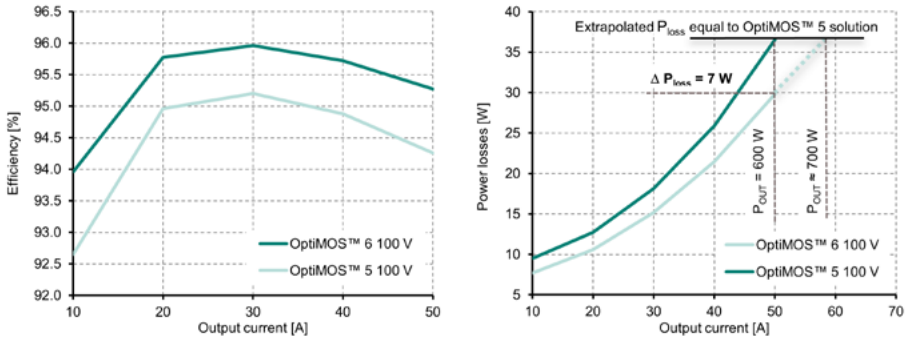

Figure 6: Efficiency and loss comparison in a 600 W ZVS inverting buck-boost topology (V_{IN} = -48 V, V_{OUT} = 12 V, f_{SW} = 200 kHz)

The performance of the latest OptiMOS 6 200 V technology under hard-switching conditions is investigated in a motor drive application. The modified, commercially available inverter – sized to drive a 65 kW AC induction motor – employs a common B6 topology with a nominal input voltage of 144 V, an average current output of 135 A_{rms}, and a 1-minute phase RMS output current of 500 A_{rms}.

The power board contains 96 MOSFETs overall in the standard TO-263-3 (D2PAK) package with 16 devices paralleled in each leg, using an insulated metal substrate power base for superior heat transfer with increased reliability and performance.

Family	Device	On-state resistance
OptiMOS™ 6	IPB068N20NM6	6.8 mΩ
OptiMOS™ 3	IPB117N20NFD	11.7 mΩ

Table 2: Best-in-class on-state resistance of OptiMOS™ devices

Parameter	Value
Switching frequency	10 kHz
Dead-time	~1 µs
Motor load phase current	160 Arms

Table 3: Test conditions

Figure 7 presents the overall mean losses per MOSFET as well as the separate conduction, turn-on, and turn-off losses. The overall loss reduction accounts for a remarkable 36 percent, with all loss contributors lowered compared with the predecessor generation. In addition, this application benefits from the much lower threshold voltage variation of the OptiMOS 6 devices because this supports a balanced current sharing. Further, this significantly improved performance does not degrade the EMI behavior, as indicated in figure 8 by the radiated emission measurement according to the applicable standard EN 12895.

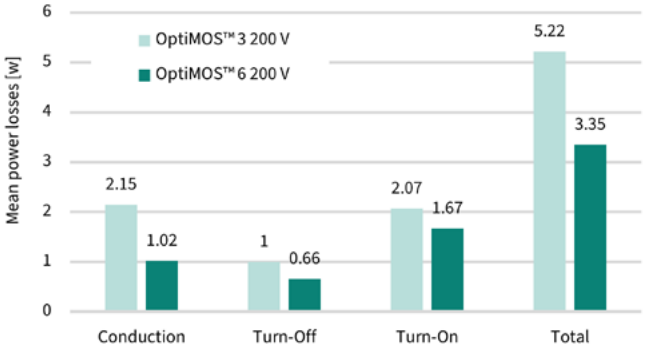

Figure 7: Comparison of mean power losses/MOSFET

This article introduces Infineon's latest power MOSFET technology family. The new generation with the latest OptiMOS technology delivers improvements in all important device parameters and combines the benefits of low on-state resistance with a superior switching performance. The remarkable progress in the overall device performance is enabled by substantial improvements at the device technology level. This has culminated in a unique device structure, which is the first to employ three-dimensional charge compensation combined with a gate grid and the first ever use of a metal gate in

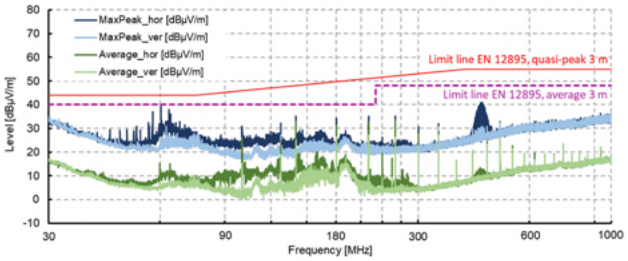

Figure 8: Measurement of radiated emission in a motor drive inverter with the new OptiMOS™ 6 200 V devices

a trench power MOSFET. The new design provides an unmatched homogeneity of the gate and field-plate resistance across the chip, enhancing the system efficiency in tested applications across all load conditions by:

- Reduction achieved in the on-state resistance
- Dramatically lowered total gate charge
- Low gate-drain charge together with a low output charge
- Improved switching homogeneity across the device area

Scan the QR code to learn more about how to bring your design to the next level of system efficiency with the OptiMOS 6 power MOSFET family.

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Using GaN FETs with Controllers and Gate Drivers Designed for Silicon MOSFETs

Gallium Nitride (GaN) FETs have revolutionized the power electronics industry, offering advantages such as smaller size, faster switching, higher efficiency, and lower costs compared to traditional silicon MOSFETs. However, the rapid evolution of GaN technology has sometimes outpaced the development of dedicated GaN-specific gate drivers and controllers. Consequently, circuit designers often turn to generic gate drivers designed for silicon MOSFETs, necessitating careful consideration of various factors to ensure optimal performance.

By Alejandro Pozo, Ph.D., Senior Applications Engineer, Efficient Power Conversion

This article explores the key differences between GaN FETs and silicon MOSFETs, provides recommendations for using generic gate drivers with GaN FETs, and outlines essential modifications for half-bridge gate drivers and controllers.

Main differences between GaN transistors and Si MOSFETs

eGaN® FETs, exhibit distinct characteristics compared to silicon MOSFETs, impacting their operation with gate drivers designed for the latter. Some of the key differences include:

a. **Lower Gate Voltage Levels:** eGaN FETs from EPC require a gate voltage of 5 V for turn-on and 0 V for turn-off, with a maximum gate rating of 6 V. This necessitates power supplies driving gate drivers to be designed accordingly. The UVLO of the driver or controller should also align with a 5 V gate drive.

b. **Faster Switching Speed:** Si MOSFETs may have more than 3x $R_{DS(on)}{\cdot}Q_G$ compared to GaN, and up to 10x higher $R_{DS(on)}{\cdot}Q_{GD}$ [1]. As a result, a dv/dt of 75 V/ns or higher may be present on the switch node, so gate drivers need to be immune to such slew rates. Faster switching speeds also make parasitic inductances more noticeable, so employing low inductance layout techniques is required in the design.

c. **Higher Reverse Conduction Voltage Drop:** Unlike silicon MOSFETs, eGaN FETs lack a parasitic body diode, but they do conduct current in reverse with a larger voltage drop; ~2.5 V [1] compared to 1 V for MOSFETs, which means the gate driver can see a higher negative switch node voltage during dead-times for the rectifying switch. Therefore, the gate driver should include bootstrap overvoltage management and be capable of operating with negative switch-node voltages down to -5V.

d. **Physical structure:** eGaN FETs have a lateral structure [1], while Si MOSFETs rated > 20 V are typically vertical devices. Consequently, the pin locations may differ, posing layout challenges when using Si MOSFET-specific gate drivers. GaN-specific gate drivers are designed to be layout compatible with most GaN transistors. Layout conflicts when using a MOSFET driver for a GaN FET require an understanding of the trade-offs that can be made in a design.

MOSFET Gate Driver Compatibility Review

Before a MOSFET gate driver can be designed to drive GaN FETs, it must meet certain requirements.

1. **Compatibility with a 5V Supply:** The gate driver must be compatible with a 5 V supply for the driver stage, either from an external regulated supply or an internal Low Dropout Regulator (LDO).
2. **UVLO Compatibility:** Under Voltage Lockout (UVLO) must be compatible with a 5 V driver stage. A typical UVLO for the low side driver stage would be between 3.75 – 4 V and 3.25 - 3.75 V for the high side.
3. **Slew Rate Immunity:** Gate drivers should exhibit slew rate immunity exceeding the maximum expected dv/dt in the switch node, preferably greater than 50 kV/µs. If this requirement cannot be met, the switching speed may need to be reduced at the expense of lower converter efficiency.
4. **Bootstrap Power Supply:** Many MOSFET drivers use a bootstrap circuit to power the upper device driver and most use a bootstrap diode. Only gate drivers that use an external bootstrap diode are suitable for use with GaN FETs as will become apparent in the recommendations. Drivers that include an LDO post the bootstrap diode are the preferred choice.
5. **Dead-time Capability:** The outstanding switching characteristics of eGaN FETs enable operating conditions in the MHz range while maintaining high converter efficiencies. Because of this, minimizing the dead time, even below 10 ns becomes very beneficial. Some controllers designed for MOSFETs will not be capable of such low dead-times thus negating the benefits of GaN devices. When considering controllers for use with GaN FETs, prioritize those with low dead-times capabilities.

Steps to Convert a MOSFET Driver to work with GaN FETs

Once a compatible MOSFET driver has been identified, then the following steps can be implemented to ensure highest compatibility with GaN FETs. Refer to figure 1 for details with the accompanying explanations. *General GaN FET driving recommendations [1] should always be followed in addition to these recommendations.*

1. **Bootstrap Diode:** For an external bootstrap diode, use the smallest possible size, capacitance, and current rating Schottky diode, such as a BAT54KFILM [2], and connect it in series with a current limiting resistor as shown in Figure 1 (a). The Schottky diode ensures the lowest loss in voltage (V_{boot}-V_{sw}) thus maintaining the driver voltage as close to 5 V as possible. The small series resistor limits the current in the bootstrap diode when any of the protection circuits kick in. It should be noted that this resistor may have an impact in the minimum pulse width required to recharge the bootstrap capacitor. Drivers with an integrated 5 V LDO after the bootstrap diode do not require the series resistor or additional circuit protections subsequently presented as those recommendations become optional.
2. **Bootstrap Clamp:** A Zener diode across the bootstrap capacitor may be used to clamp the voltage to below 6 V to prevent over-

voltage during dead-times with the low-side device in reverse conduction. A good example would be MM5Z5V6ST1G [3] with a Zener voltage of 5.6 V as shown in Figure 1 (b). Both the bootstrap capacitor and Zener diode should be placed as close as possible to each other, and as close as possible to the gate driver.

3. **Gate Return Resistor:** Adding a gate return resistor, as shown in Figure 1 (c), for the high side FET can protect the IC from a large negative voltage on the switch node during reverse conduction of the low side GaN FET as shown in Figure 2. The value of this resistor also depends on the turn-off damping and timing needed for the upper device gate circuit. Using this resistor requires an equivalent reduction in the turn-on resistor for the gate to compensate for its resistance.

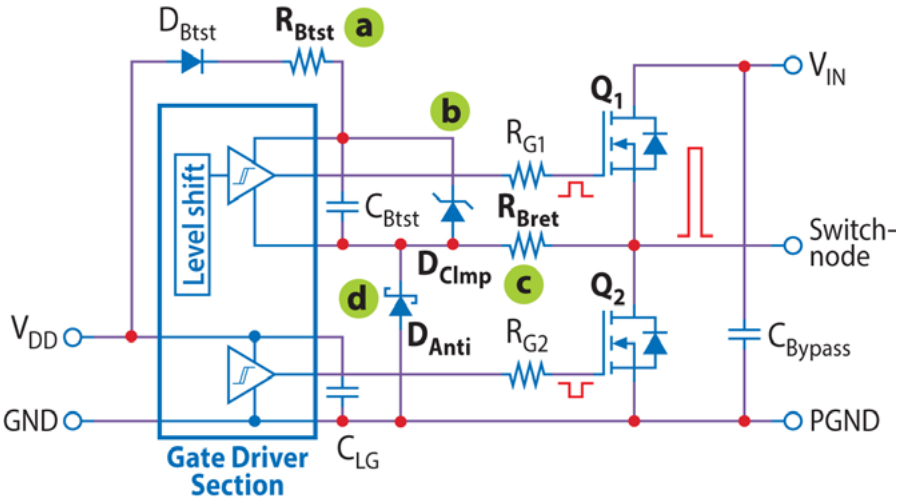

Figure 1: Recommended Si Gate driver augmentation for GaN FET compatibility.

4. **Reverse Conduction Clamp:** An anti-parallel Schottky diode across the low side of a half-bridge topology, as shown in Figure 1 (d), can limit the magnitude of negative switch node voltage the driver is exposed to. Some gate drivers become sensitive to or may even fail when the switch-node falls below certain voltages below the ground reference [4]. The voltage rating of this diode should match that of the low side GaN FET. The current rating can be significantly lower than that of the low side FET because it only conducts during dead times, so it should be selected based on its pulsed current rating.

Working with Controller ICs with Integrated Gate Drivers

Controller ICs integrate many functions into a single IC, including the gate driver [5-7]. Some of these ICs may not allow an optimal layout for GaN devices, so it is important to understand the design compromises that can be made to achieve the best performance.

When designing a power stage using GaN FETs, it is important to always follow the general layout recommendations provided in [8, 9]. The order of consideration remains common-source-inductance (CSI), followed by the power loop and then the gate loop inductance [10]. This means that the power stage is essentially designed as a block and then the gate signals connected to the controller IC as shown in Figure 3. Variations of the recommended layout for the power stage block are given in [11] making it easier to choose an optimal block that can fit the controller IC. In the case of 2-phase controllers, it may be necessary to choose between 2 alternative designs. The design criteria is to prioritize

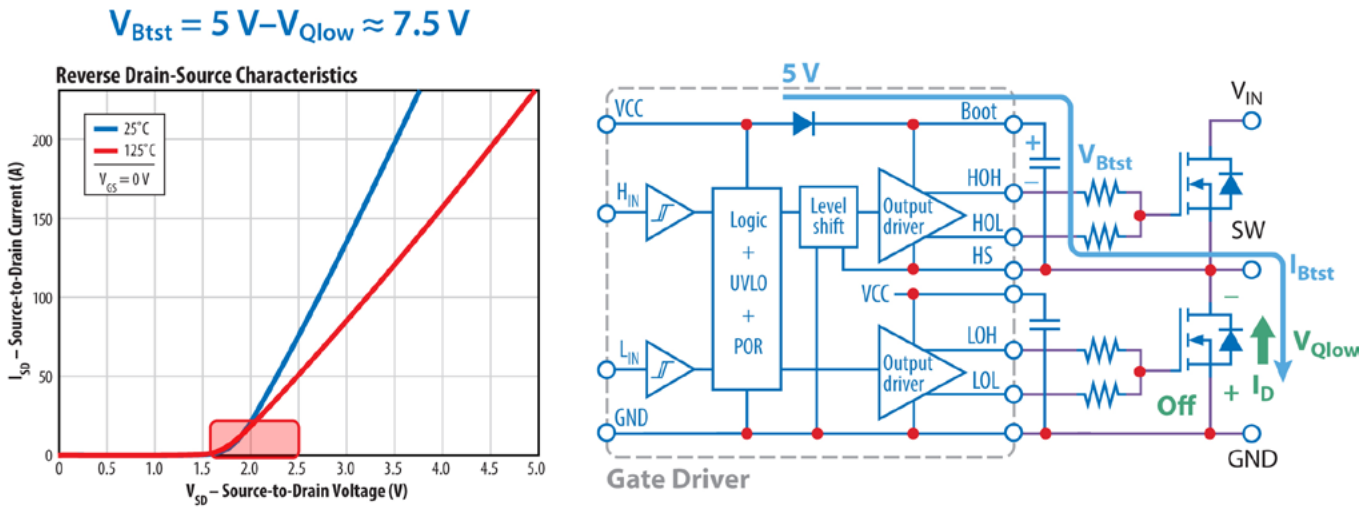

Figure 2: Bootstrap charging path during dead time.

the control FET (switch), which is typically hard switched, over the synchronous rectifier. For example, in a buck converter, the layout should be optimized to minimize parasitic inductance in the gate loop of the high side FET. The same would be true for the low side FET in a boost converter as shown in Figure 3.

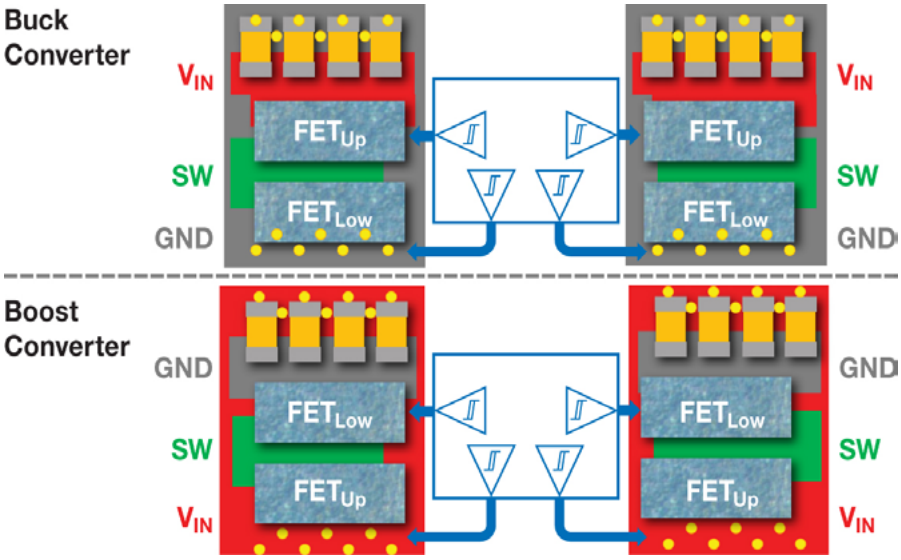

Figure 3: Recommended layouts.

Conclusions

This article presents a method to adapt MOSFET gate drivers for use with GaN FETs. Designers must ensure compatibility, implement recommended modifications, and optimize layouts to harness the full potential of GaN technology. With careful attention to these guidelines, designers can use generic gate drivers and controllers, paving the way for successful high-volume production of GaN-based power converters.

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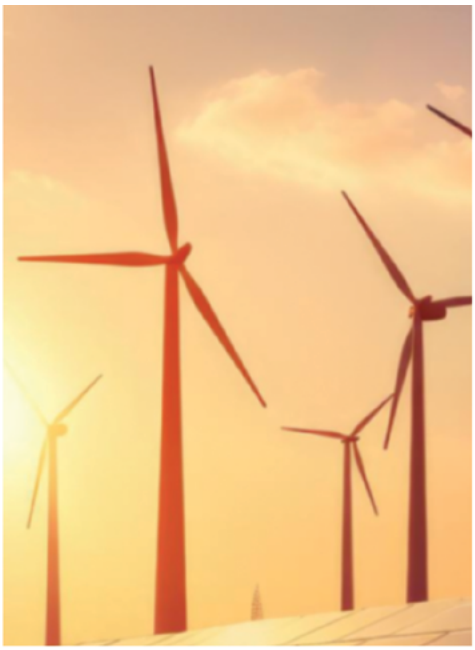

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Double Pulse - Thoughts of a Test Equipment Manufacturer

Over the last 20 years, I have heard many - sometimes amusing - explanations for the double pulse. For example, "the double pulse is the characterisation of an electrical quadrupole, with the first pulse describing the input and the second pulse the output". What is self-evident for the experienced professional can sometimes cause misunderstandings for the less experienced. As a test equipment manufacturer, realised that users have different perspectives of the topic of double pulse testing.

By Dipl. Ing. Konrad Domes, CEO, SAXOGY POWER ELECTRONICS GmbH

The development of a power electronic assembly requires several steps. One of these involves the dynamic characterization of the switching behaviour of the power semiconductors. For this purpose, a double-pulse test setup is used which includes:

- a capacitive energy storage device, also known as dc-link capacitor,
- the power semiconductors that are to be tested, which consist of at least one switch and one diode, and
- a load inductor, which functions as a magnetic transducer.

The IEC 60747-9 standard explains the corresponding test setup and the measurement results using the example of an IGBT. As expected, no further details are given about the real designs and possible pitfalls.

What is the double pulse actually used for?

The schematic of a possible double pulse setup is displayed in picture 1, with the measurement data in picture 2.

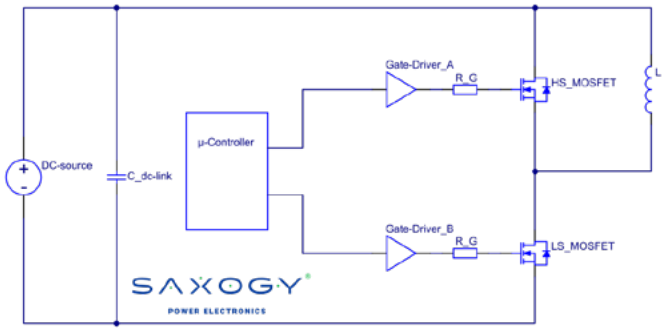


Figure 1: Basic double puls setup including two MOSFET

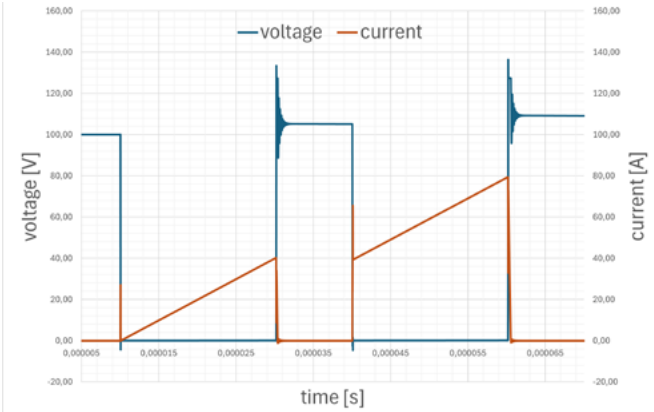
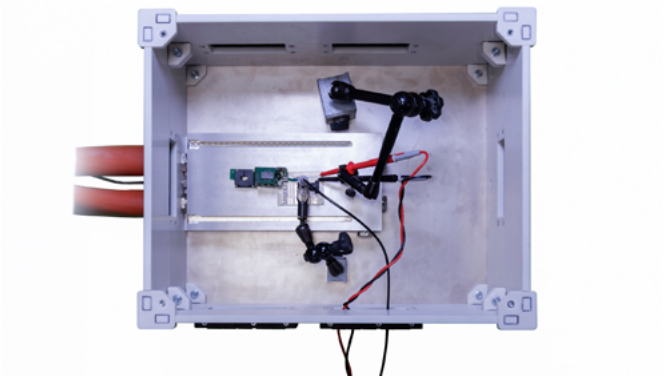


Figure 2: Simulation results of a double puls setup

With a first pulse, the load inductance is magnetised up to the desired rated current, whereby switching off the current provides the first data (A) on the switch-off behaviour at the operating point. After a recovery time, during which the semiconductor must be completely de-energised, it is switched on again. The previous nominal current flows - driven by the load inductance - in the opposite diode. When switched on again, the current commutates back into the semiconductor that is being tested.

This provides the second data set (B) with all the information about the turn-on behaviour of the power semiconductor. Once the turn-on process under nominal current has been fully recorded, the second pulse is switched off. However, the resulting data are not necessarily of interest.

In general, it is assumed that a semiconductor that survives a switching operation at a specified operation point without any problems, will always survive this operation point. Provided the semiconductor does not degrade and the resulting heat is continuously dissipated. The required cooling capacity can be calculated by characterising all plausible operation points and by calculating the power losses, considering the switching frequency.



Fiure 3: SAXOGY´s double puls test box with temperature management and inert gas connections

Parasites – invisible but meanly

In addition to the load inductance, each piece of connecting cable introduces a further amount of inductance into the circuit. Unfortunately, this also occurs in areas where there should be as little as possible or no inductance at all. Additionally, each piece of cable forms a coupling capacitance to neighbouring conductors. These parasitic passive components in turn form resonant circuits, which can easily be triggered by fast-switching components.

Of course, all distances between the components should be as short as possible. The commutation circuit, which is formed by the two semiconductors and the dc-link capacitance, can thus be reduced to inductance values of approx. 10 nH.

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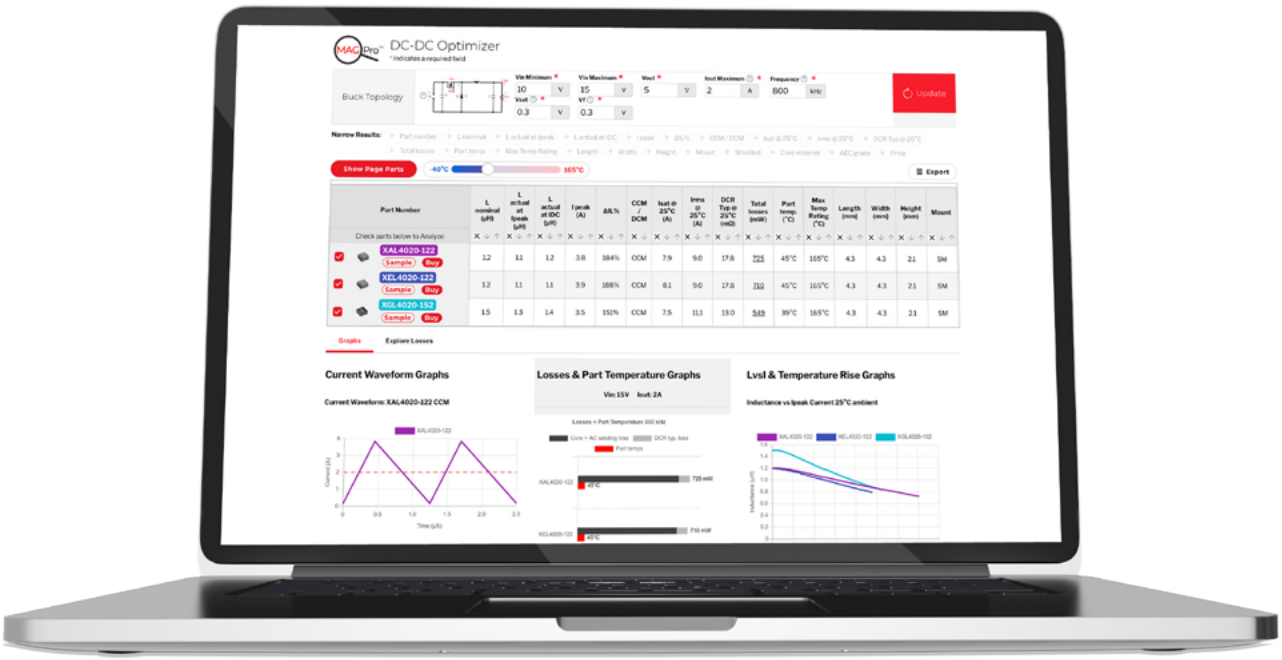

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After the turn-off, the corresponding semiconductor turns off by building up a junction barrier. The junction-capacitance forms a resonant circuit with the commutation inductance. The resulting turn-off oscillations can be recognised as an overlap on the reverse voltage curve. The turn-off process interrupts the current flow in the commutation inductor, causing it to generate a turn-off overvoltage.

Depending on the setup, the overlap of turn-off overvoltage and turn-off oscillation can lead to an increase or partial cancellation of the peak voltage value. To prevent the maximum reverse voltage on the semiconductor from being exceeded and the associated destruction of the semiconductor, the turn-off behaviour should be characterised under worst-case conditions. These include the use of the future target layout, the expected junction temperature with the highest switching speed and the turn-off at the highest current.

Experience shows that critical conditions sometimes occur even at operating points between the maximum values. For this reason, close characterisation of the switching processes over the entire operating range is recommended.

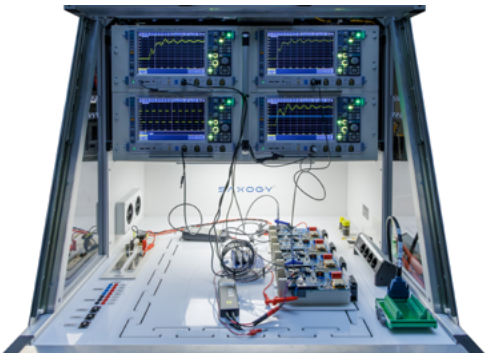

Figure 4: SAXOGY´s fully automated double puls test bench with included measurement equipment

The right sequence saves time

Here, a fundamental distinction must be made between characterising the semiconductor and characterising the power electronics.

Load current

The easiest and fastest way to obtain data is to modify the operating point of the current. The current to be switched off is related to the turn-on time. There are two issues to be considered:

a. The current-carrying load inductance has a certain energy amount that was provided by the dc-link capacitance until turn off.
b. Energy was lost during the turn on phase due to conduction losses. As a result, after turn-off the dc-link capacitance no longer has the same voltage value as when it was switched on.

To switch off at a specific voltage value, the dc-link voltage must therefore be increased by the expected difference. The current range should consider all values that occur during operation - especially short circuit events.

The range between two operating points is debatable: 5 to 10 operating points within the rated current range are common. Of course, a fully automatic test bench allows a more closely meshed characterisation. Fortunately, the days when every measurement plot was saved on a disc or evaluated with a lot of manpower are long gone...

Gate configuration

Some setups offer the option of manipulating the way in which the gate driver is controlled. For example, gate resistors, gate currents or gate voltages can be adjusted automatically. As these have a direct influence on the switching behaviour, those must be considered during the characterisation. Often only seconds are needed to re-parameterise the gate driver. It is therefore recommended - after each operating point or at the end of a series of operating points with the same dc-link voltage - to include the new parameter in the characterisation.

However, if the gate driver is not automated, manual parameterisation should be carried out at the end of the entire measurement series. As the test system must be disconnected from the power supply after each pulse and the statistical number of accesses is therefore significantly higher than when parameterising a complete series, this significantly minimises the safety risk. Characterisation over the entire current range is now repeated for different dc-link voltages. To save energy and time, it is advisable to characterise several current values with the same dc-link voltage. This avoids unnecessary charging and discharging cycles of the dc-link capacitor.

Dc-link voltage

The voltage range limitations for semiconductor characterisation are between zero and usually 80% of the maximum permissible reverse voltage. The turn-off overvoltage must never exceed the maximum permissible reverse voltage!
When characterising power electronics, for example, it is possible to limit the characterisation parameters to the voltage range of the inverter. Usually, all voltage ranges are measured with at least 5 to 10 intermediate points, whereby, again, a more detailed characterisation provides more insight.

Junction temperature

The junction temperature is usually the last parameter to be modified. Several different methods are possible. The easiest way to control the temperature is to use a heating plate, where the semiconductor or the heat sink is heated up to the desired temperature. With this method, however, only junction temperatures above room temperature are possible.

An extension of the process is the temperature regulation by means of a hydraulic temperature control plate. In principle, this is an oil-filled heat sink. The temperature of the oil is controlled by a temperature control unit. With this setup temperature ranges between -40°C and +200°C are possible. It should be noted that at temperatures below the dew point, condensation and later icing of the device under test (DUT) can occur. In turn, metallic surfaces can oxidise at high temperatures. Ideally, the DUT should be operated in an inert gas environment. The moisture and oxygen-free environment prevents both icing and oxidation.

To summarise, it can be said:

Of course, these few words can only provide a rough overview on this topic. The double pulse probably offers enough material to write an entire book. Our aim is to look at important aspects of the double pulse in more detail in the following issues. I hope that this short treatise will increase the number of double pulse engineers and that even more reliable solutions will be created in the future.
Anyone who does not feel confident enough to tackle the subject in such depth but still needs results is welcome to get in touch with us. We at SAXOGY® have a whole series of predefined solutions. If you cannot find what you are looking for, we will be happy to develop a customised solution.

About the Author:

Dip. Ing. Konrad Domes: Studied electronics and electrical engineering at Chemnitz University of Technology; Worked as a development engineer and head of the Chemnitz branch for power electronics at the Fraunhofer IISB; Experience in analog circuit technology, gate drivers, current sensors, double pulse, power electronics, HVDC, test benches; Teaching position at Chemnitz University of Technology; Since 2004: Konrad Domes Engineering Office
Since 2018: Managing Director/CEO SAXOGY POWER ELECTRONICS GmbH

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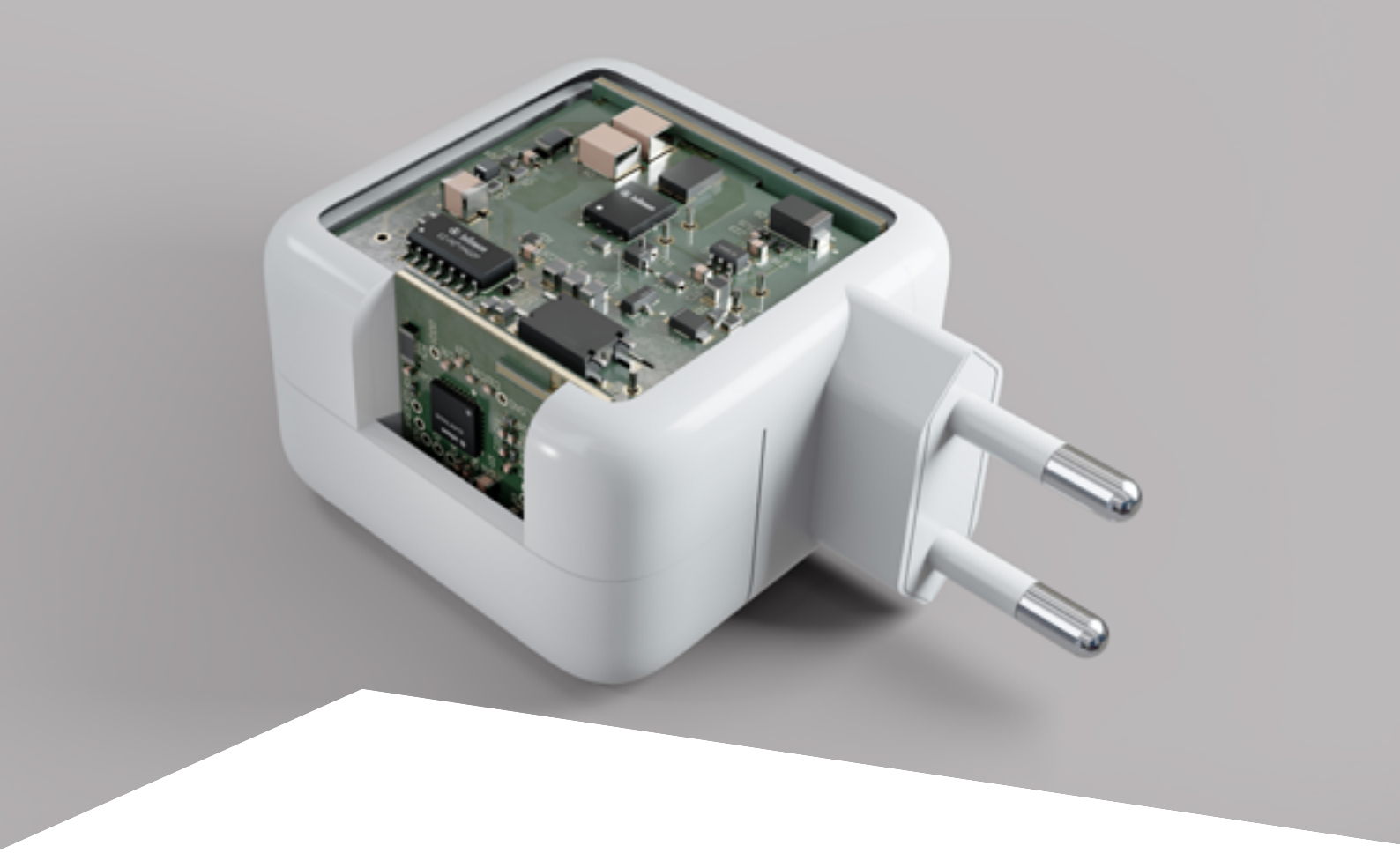

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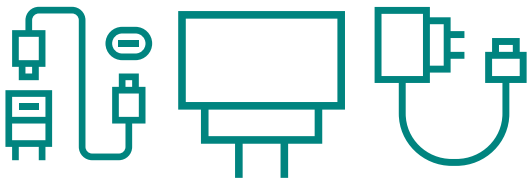

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Accelerating Mobility Electrification Beyond Cars with Modular & High Power SiC Traction Inverters

Freight transportation, off-road and industrial vehicles, marine applications and aviation contribute more than 55% [1] of the total greenhouse gas emissions from internal combustion engines. Electrifying these powertrains could make a large difference in the fight against climate change. However, the large quantity of units in action worldwide is associated with a wide diversity of types and platforms.

By Pierre Delatte, CTO, CISSOID

To develop new electric drives quickly, engineers need all the help they can get. The differences are more than simply physical, in terms of size, shape, and weight constraints. The functional and electrical safety requirements, and environmental conditions, are highly dependent on applications and geographical markets. On the other hand, the competitive situation between all manufacturers demands a fast time to market.

For performance and reliability, silicon carbide (SiC) is the power semiconductor technology of choice. While range-anxiety is one issue that has moved the passenger car market away from silicon and towards more energy-efficient SiC, vehicles such as buses operate on known routes and off-road vehicles cover relatively short distances. For these applications, SiC's high-voltage capability permits faster charging for shorter turnaround times, and its ability to operate at high temperature helps maximise reliability. Moreover, modules require fewer SiC devices to share the duty, and SiC MOSFETs can be smaller in relation to breakdown voltage than their silicon counterparts. Hence, savings in module size are also possible.

However, SiC power devices are not a direct drop-in replacement for silicon MOSFETs or IGBTs. Arranging proper control of the gate to ensure fast and smooth switching transitions at high frequency is not straightforward. There are further challenges including integrating hardware components, especially the inverter and the intelligent power module, and setting up and calibrating the motor-control software.

Figure 1: CISSOID's high-voltage SiC inverter reference design.

Accelerated Development

To help overcome the development challenges and accelerate time to market for robust and reliable SiC power modules (Figure 1), CISSOID has produced a SiC traction-inverter platform and reference design. Drive makers can use this to build systems capable of operating from battery voltages up to 850V. The hardware is modular and scalable to produce designs of various power ratings.

The reference design solves aspects of the inverter that are notoriously difficult and time-consuming to get right. The core components include a 3-phase 1200V intelligent power module (IPM), already integrated with a gate driver optimised for SiC applications and designed to withstand elevated temperatures (Figure 2). The driver provides peak gate currents in excess of 10A and can operate in ambient temperatures up to 125°C.

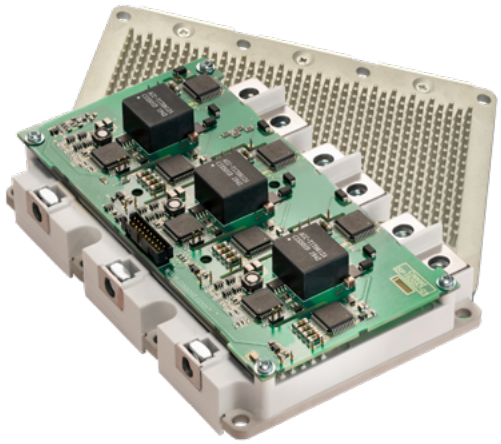

Figure 2: The Intelligent Power Module (IPM) comprises SiC power stage with pin-fin cooling and top-mounted gate driver [2].

Because the SiC gate driver is already integrated with the power module, users can start their projects with a solution that is already validated and optimised for fast switching speed and low losses, immune to high dI/dt and dV/dt effects, and that contains robust protections for the power stages. As a result, the number of iterations required to fine-tune module performance and ensure proper thermal management is significantly reduced. Additional hardware in the reference design includes DC-current and phase-current sensors, EMI filtering, a compact liquid cooler and high-density DC-link capacitor. The DC-link capacitors are specifically developed for the inverter platform and cover a broad range of voltage and current options.

Software Control and Calibration

To complete the reference design, there is also an e-motor control board, with an application specific processor and software, both pre-certified to the ISO 26262 standard, ASIL level D for functional safety. The motor control software allows a wide range of adjustments without compromising the functional-safety certification, giving flexibility to optimize the motor behaviour as required in the end use case. The users can run their own custom application software on top of this.

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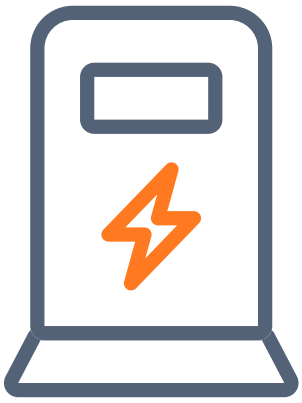

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The control board is designed around the Silicon Mobility OLEA® T222 field-programmable control unit (FPCU). This approach allows the reference design to combine the software-based flexibility of a conventional processor with hardware acceleration to ensure real-time performance up to the highest desired motor speed. By including the control board, the reference design also helps users to avoid the usual mechanical and electrical integration challenges when bringing the control board and Intelligent Power Module together.

The OLEA® APP INVERTER is a flexible and fully customisable control software (Figure 3), that matches any electric powertrain configuration and power range thanks to a set a configuration and calibration parameters that can be modified either offline or in real-time. The software also comes with a debugging and calibration framework including a graphic interface.

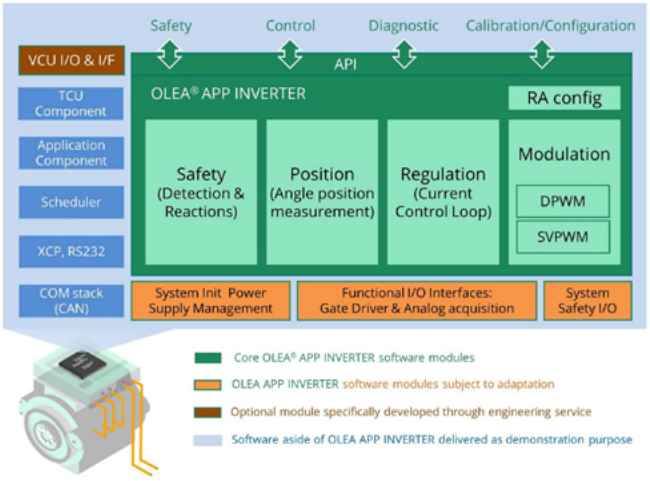


Figure 3: The OLEA® APP INVERTER control software provides multiple features to regulate and optimise motor operation.

Using OLEA® COMPOSER, developers can shorten the time required to optimise the motor control software (see sidebar for more information on the four-step process to accomplish this).

SiC Inverter Performance

After the parameters are set up, the motor can be tested and the efficiency of the inverter-motor combination can be mapped. Figures 4a and 4b compare the performance of the SiC-based inverter with a silicon-IGBT inverter tested under similar real-world conditions.

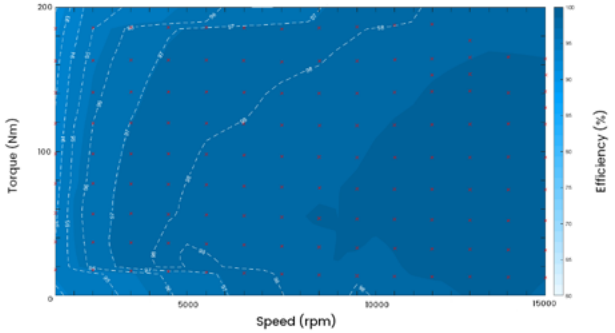


Figure 4a: SiC inverter performance up to 260kW @ 13500rpm, showing efficiency across speed and torque range.

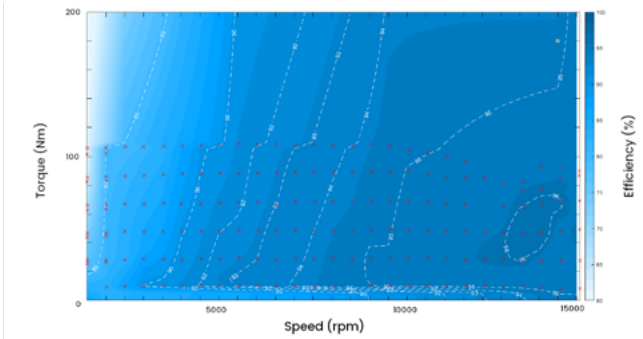


Figure 4b: The silicon-based inverter up, to 120kW @ 11500rpm, has impaired torque capability (see cross-points) under comparable conditions.

Setting up and Calibrating the Drive

The OLEA® COMPOSER tools suite helps the user get the motor spinning according to the customer's specifications. It assists in performing calibration of parameters such as voltage, power rating, speed, and torque to reach an optimal working range. Once this is complete, the inverter-motor efficiency can be mapped.

Setup and calibration are completed in four steps:

Step 1: Software parameters configuration

- Configuration of the OLEA® APP INVERTER software according to the e-motor parameters.

Step 2: Inverter hardware setup

- Setup of e-Motor including components such as resolver and temperature sensors. Connection of EV electronic control unit (ECU) and bench (e.g. CAN, safety) interfaces, power and cooling interfaces.
- Check inverter safety interfaces with the test bench.

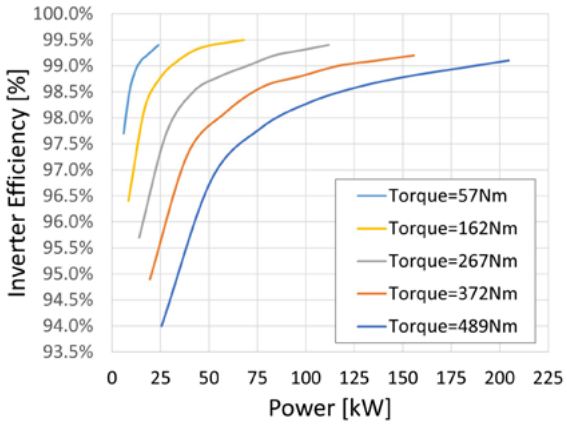
Step 3: Motor-control system calibration

- Open loop mode: calibration of current and voltage sensor signal conditioning chains by the OLEA® T222 FPCU.
- Partial open-loop mode: position sensor offset calibration, whether using resolvers or inductive sensors.
- Current closed-loop mode: internal PI controller tuning of ID and IQ vectors for field-oriented control (FOC).
- Torque control mode: fine-tuning of torque control loop for precision and dynamic response.
- Speed closed-loop mode: speed regulator calibration.

Step 4: Advanced System Optimisation

- Scaling of switching frequency: adjustment of the switching frequency depending on speed and phase currents.
- Dead time compensation: adjustment of the deadtime compensation algorithm to minimise the phase-current harmonics.
- Flux Weakening: ID/IQ setpoints optimisation for an efficient operation in the maximum torque per voltage (MTPV) region.
- SVPWM/DPWM: definition of the threshold between space vector pulse-width modulation (SVPWM) and discontinuous pulse-width modulation (DPWM), offering higher efficiency at high speed.

Using this approach allows tuning of the reference design to achieve efficiency greater than 99%, operating on a 700V bus, up to 4000rpm, as shown below:



These performance plots show how the greater efficiency of the SiC-based drive ensures a superior user experience. With increasing speed and load demand, the motor torque when operating from the IGBT-based drive, becomes significantly reduced owing to its lower efficiency; the self-heating associated with the energy losses in the device cannot be dissipated without greatly increased cooling. In contrast, the highly efficient SiC-based drive can deliver closer to the maximum torque over a much wider speed and load range.

Conclusion

The bus, truck and agricultural vehicles sectors present a good opportunity for electrification and for reducing the emissions burden on the environment. Silicon carbide power technology can help maximise both reliability and vehicle duty cycle, as well as delivering superior efficiency compared to silicon IGBTs or MOSFETs. The complexities of designing with SiC, and the imperative to ensure a fast time to market, demand a flexible development platform to help designers satisfy the targets for various vehicle categories and types. A complete reference design that offers solutions to the main challenges when designing with SiC, while also allowing flexibility and scalability to address different power ratings and battery voltages to handle small to large vehicles, effectively minimises design risks and helps accelerate time to market.

References

[1] Source: NESTE: Towards sustainable mobility / April 2023: https://journeytozerostories.neste.com/transportation/towards-sustainable-mobility#885e75ed

[2] CISSOID SiC Intelligent Power Modules: https://www.cissoid.com/sic-power-modules/

https://www.cissoid.com/tools/reference-designs

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Application Advantages of Intelligent IGBT Gate Drivers in 3300Vac Coal Mine Inverters

In recent years, the coal mining industry has re-entered a period of rapid development, the demand of the core equipment for coal mining, 3300Vac high power inverters is growing. Due to the harsh environment of the coal mine, such as small space and inconvenient maintenance, the demands of high reliability, miniaturization and intelligence for the inverters are put forward.

By Lei Hong, Product Manager HV Gate Drivers, Hangzhou Firstack Technology

As the core components of the inverters, IGBT and gate driver play a crucial role. At the early stage, IGBT gate drivers in the industry were dominated by imported analogue gate drivers. As the development of digital gate driver technology is mature, the demands of high reliability, miniaturization and intelligence can be better satisfied, the application is more and more widespread. According to the NPC I-type 3-level topology characteristics and application challenges of 3300Vac inverters, Firstack targeted developed a new generation of intelligent IGBT gate drivers, which can effectively solve the problems of the incorrect turn-off timing of the inner and outer IGBTs, too high turn-off overvoltage of inner IGBT, and the large turn-off delay time of high-voltage IGBT module, etc. Additionally, the IGBT gate drivers can satisfy the intelligent needs of maintenance by the intelligent fault communication technology.

Introduction

The 3300Vac coal mine inverters, as is shown in Figure 1, is mainly used for heavy-duty soft starting and intelligent speed regulation of coal mine scraper conveyor, belt conveyor and transfer machine. Its power ranges from 500kW to 2600kW[1], which belongs to high-voltage high-power power electronic equipment. The main topology scheme is the NPC I-type 3-level with the 4500V IHV IGBT package module, as is shown in Figure 2.

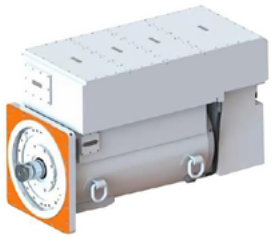
For NPC I-type 3-level applications with high-power IGBT, there are challenges following at the level of IGBT module and gate driver technology:

The problem of turn-off timing of the inner and outer IGBTs in any case, the outer IGBT has priority over the inner IGBT to turn off, especially in the case of short-circuit fault or undervoltage fault. The Vce short-circuit protection time of the traditional analogue gate driver is too long, which leads to the inner IGBT under short-circuit condition withstanding a long short-circuit time that exceeds the safety range. In other words, there is a great risk.

Too high turn-off overvoltage of inner IGBT: Since the topology is more complex than the traditional 2-level topology, there is a large commutation loop in the inner IGBT, and the actual high-power module design has a large stray inductance in the busbar, which can easily lead to the module damage due to the high turn-off overvoltage. At the same time, in some applications, the space is very compact, part of the design can not add absorption capacitors, resulting in the turn-off overvoltage more of a problem.

Large switching delay for high voltage IGBT modules: some of the high-voltage IGBT modules have excessive switching delays, leading to great challenges in dead time setting and waveform quality control.

Figure 1: (a) 3300V coal mine inverter



(b) 3300V coal mine inverter with motor together

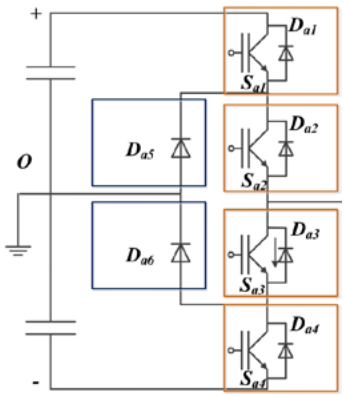


Figure 2: (a) One phase topology of the 3300 Vac inverter

(b) 4500V IHV IGBT module and gate driver

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Demand of IGBT intelligence maintenance: 3300V coal mine inverters are generally installed in the mine shaft, when there is an IGBT module has failed, whether it can quickly locate the cause of the failure is critical for reducing maintenance cost. At the same time, it is an important way to improve benefit for the equipment manufacturers to dominate the maintenance market in the increasingly fierce business competition environment.

IGBT Gate Driver Application Challenge

Turn-off timing of the inner and outer IGBTs

As is shown in Figure 3, in the NPC I-type 3-level topology, there are 6 power devices in each phase: 4 IGBTs (S_1, S_2, S_3, S_4) and 2 diodes (D_5, D_6). Different switching combinations of the 4 IGBTs can be composed of different commutation modes, and the states of S_1~S_4 are represented by 0 and 1, respectively, 0 represents turn off and 1 represents turn on. At the same time, the positive potential of the bus is "+1", the negative potential of the bus is "-1", and there are several combinations of modes (assuming the current flows inward), as shown in Table 1.

S1	S2	S3	S4	Hexadecimal	Output
1	1	0	0	C	+1
0	1	0	0	4	+1
0	1	1	0	6	0
0	0	1	0	2	0
0	0	1	1	3	-1
0	0	1	0	2	0
0	1	1	0	6	0
0	1	0	0	4	+1
1	1	0	0	C	+1

Table 1

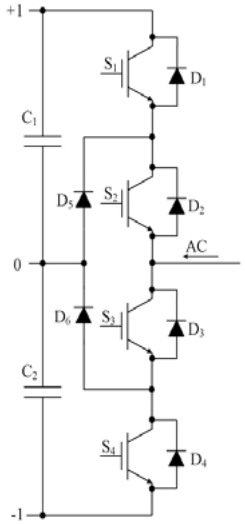

Figure 3: NPC I-type 3-level topology

As can be seen in the above table, there are 5 modes in the NPC I-type 3-level, including steady state C, 6, 3 and transition state 4, 2, where the steady state C, 6, 3 follows the principle of complementarity of S_1 and S_3, and complementarity of S_2 and S_4. In order to analyse the timing problem, mode 3 is taken, at this time the state of S_1~S_4 is: 0011, as is shown in Figure 4a, S_3 and S_4 are open, the current flows from AC to the bus negative, at this time the AC point potential is "-1". If there is a normal shut down or abnormal overcurrent, which of the inner IGBT S_3 or the outer IGBT S_4 should be turned off first?

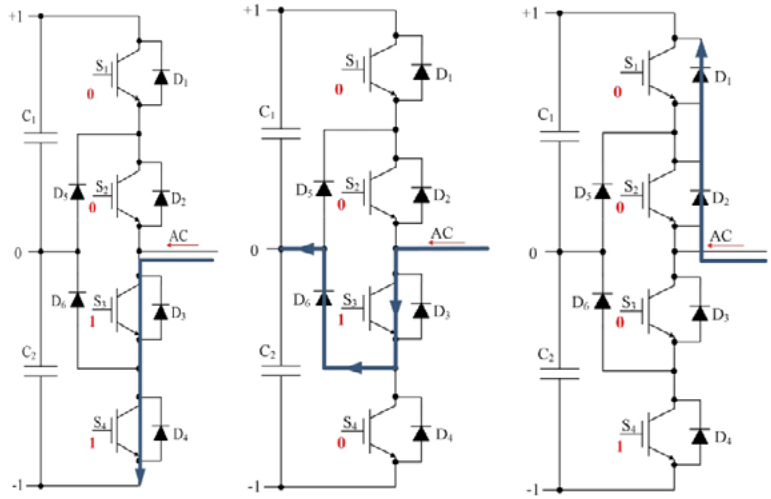

Figure 4

Figure 4(b) shows that the outer IGBT is turned off first (S_4=0), after which the current flows back to point O through D_6 and the AC potential is "0", and then the inner IGBT is turned off (S_3=0), and the inner IGBT S_3 is subjected to 1/2VDC at both terminals. Figure 4(c) shows that the inner IGBT is turned off first (S_3 = 0), after which the current flows through D_1, D_2 back to the bus positive, AC potential is "+1", and then turn off the outer IGBT (S_4 = 0), the voltage across the inner IGBT S_3 is V_{DC}, the module will damage due to overvoltage.

Based on the above analysis, the NPC I type 3-level must turn off the outer IGBT before turn off the inner IGBT, either under normal shut down conditions or under abnormal conditions. Under normal operating conditions, it is relatively easy to achieve timing turn-off through the control board. However, under short-circuit fault conditions, there are great challenges in the timing, the traditional analogue gate driver scheme (e.g., PI) is mainly based on Vce short-circuit protection and active clamping function, while assisting the master computer to coordinate the turn-off timing to complete. In this protection scheme, when there is a short-circuit fault in the inner IGBT, it will turn off first by itself, which results in overvoltage of the inner IGBT due to the turn-off timing error. But the inner IGBT active clamping function will clamp the voltage at both terminals of the IGBT, at the same time, the master computer is informed of the inner IGBT short-circuit fault. After learning of the fault information, the master computer immediately turns off the outer IGBT fitrst and then the inner to ensure the corresponding turn-off timing under the condition of the inner IGBT not overvoltage. In the above protection scheme, the traditonal driver will have the following problems.

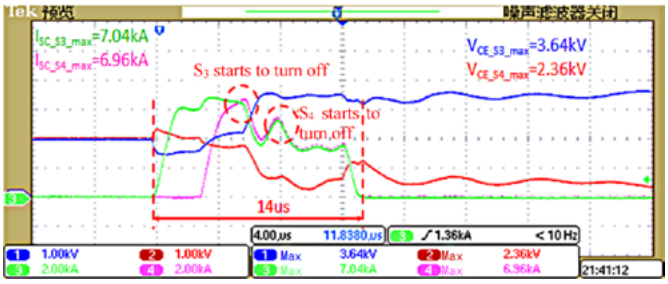

Figure 5: Short-circuit test of high voltage module with 3-level topology

First of all, due to the Vce short-circuit protection response time of the traditional gate driver is generally about 8us, in extreme cases, it will lead to the inner IGBT withstanding a long short-circuit time that exceeds the safe range under short-circuit conditions. Figure 5 shows the short- circuit condition test of PI analogue gate driver product [2] based on 4500V/1200A IHV module in NPC I-type 3-level topology. S_3 is the inner IGBT, S_4 is the outer IGBT. As is the test waveform, the outer IGBT is turned off first and then the inner IGBT, but the outer IGBT withstands the whole short-circuit time of 14us, more than the module safety limit of 10us, which means there is a great risk.

Secondly, the traditional gate driver generally uses the basic active clamping technology, and the clamping circuit has the problem of inaccurate clamping voltage, specifically shown in Figure 6(a). The basic active clamping circuit, which is directly connected to the IGBT C and the gate G through a certain number of TVS, when the IGBT is turned off, once the turn-off overvoltage exceeds the clamping threshold of the TVS, the TVS breaks down, and the breakdown current will be injected into the gate, leading to the gate Vge voltage rising and delaying the IGBT turn-off, so that the turn-off overvoltage energy will be consumed through the IGBT loss, and the turn-off voltage is clamped by the TVS. However, the actual turn-off process, the last level of push-pull circuit of the gate

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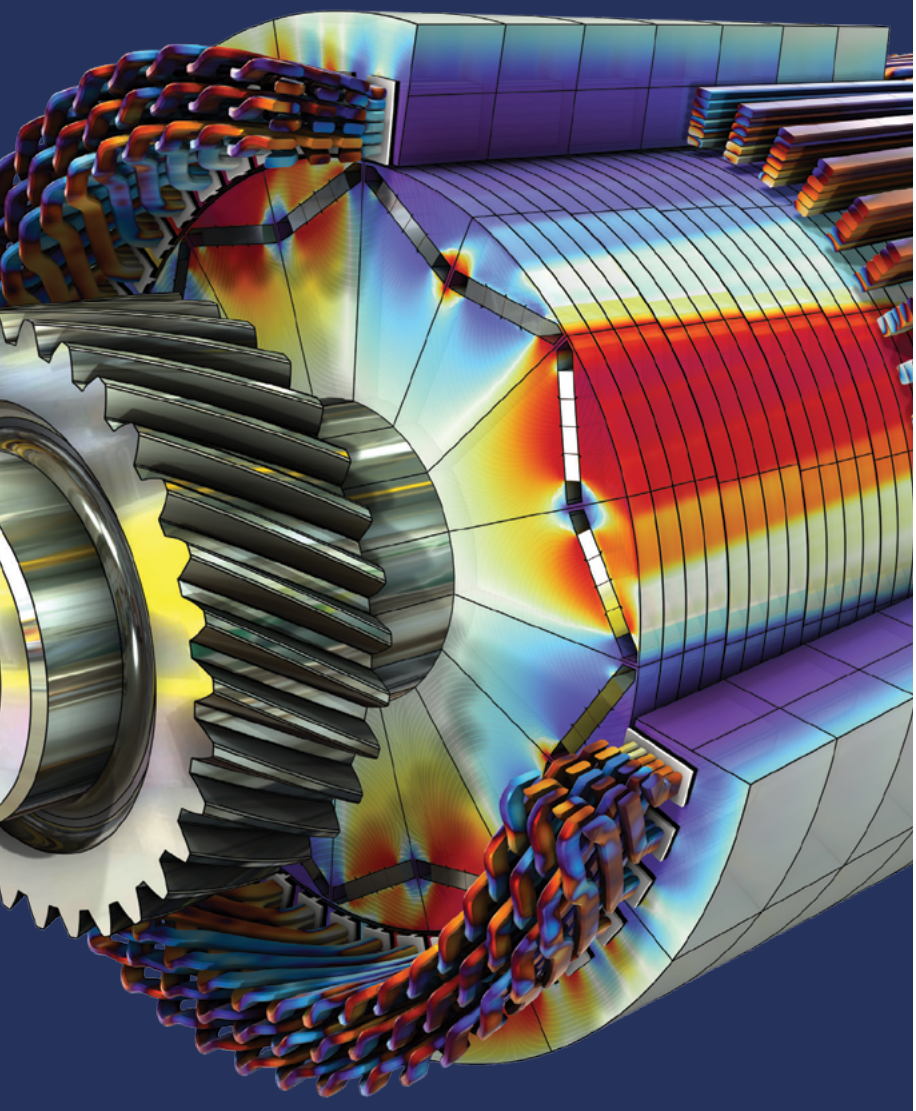

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driver is connected to the -15V power supply, for the TVS breakdown current, there is a low-resistance path, which will lead to a large fluctuation in the current flowing through the TVS. According to the TVS V-I characteristic curve, as is shown in Figure 6(b), when the current flowing through the TVS fluctuates drastically, the clamping voltage of the TVS also fluctuates drastically, resulting in inaccurate clamp voltage.

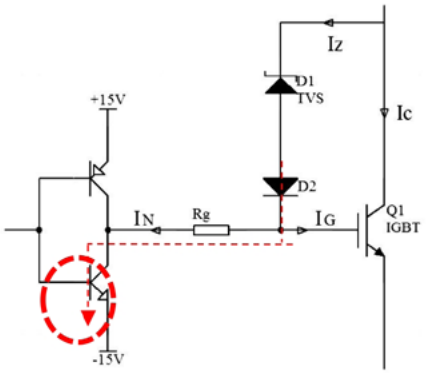
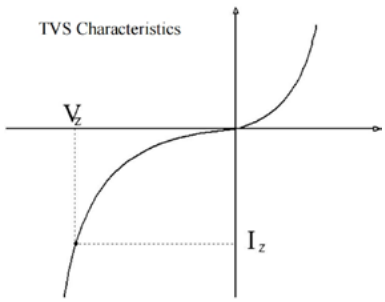
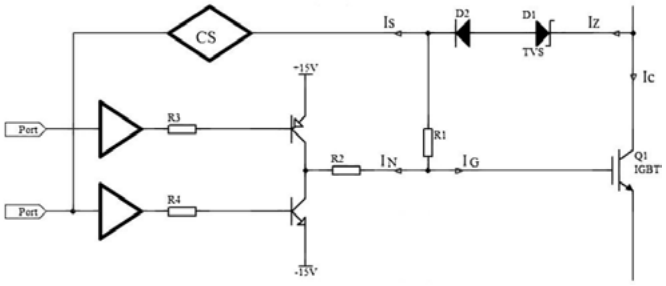


Figure 6: Basic active clamping circuit



V-A characteristic curve of the TVS

In order to solve the problems inherent in the basic active clamping technique, PI[2] introduced the dynamic advanced active clamping DA^{2}C technique, as is shown in Figure 7(a). Compared with the traditional basic active clamping technique, the current at the time of TVS breakdown is sampled via the CS circuit, and according to the current, the gate push-pull circuit is adjusted to the switching state of the -15V power supply, and when the current at the time of TVS breakdown is smaller than the set threshold, the push-pull circuit is connected to the -15V power supply. When the TVS breakdown current is larger than the set threshold, the push-pull circuit is cut off from the -15V power supply, which removes the low-resistance path. This can effectively control the TVS current, thus effectively control the clamping threshold of TVS, which makes the clamping voltage more accurate. Figure 7(b) is the test waveform under short-circuit condition for the PI analogue driver products [2] based on Infineon FF1400R12IP4 module, and the Vce voltage is basically clamped at about 750V at the turn-off moment.



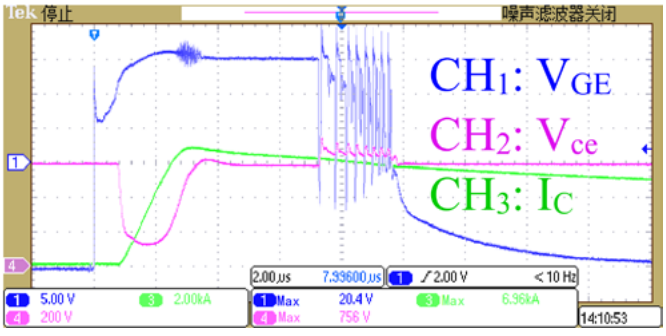


Figure 7:
Advanced active clamping circuit
Test waveform under short-circuit condition

Compared to the basic active clamping, dynamic advanced active clamping DA^{2}C can effectively suppress turn-off overvoltage, and the clamping effect is great, but the voltage clamping process will be accompanied by gate repeatedly turned on and off during a very short period of time, generating a certain amount of electromagnetic oscillation inside the module, which is a hazard for the safe operation of the module. During the actual action, the TVS current and power consumption are still large, if the active clamping circuit operates for a long period of time, the life and reliability remain a big challenge.

Too high turn-off overvoltage of inner IGBT

As is shown in Figure. 8(a), the NPC I-type half-bridge operates in mode 6, the switching state of S_1~S_4: 0110, and the current will flow from the AC point to the "O" point through S_3, D_6. At this time, switch to mode 4, that is, S_1 ~ S_4 switching state: 0100, the current will flow from the AC point through the S_2, D_1 to the bus positive, in the turn-off process of S_3, as is shown in Figure 8(b), the entire commutation circuit passes through the C_1, D_1, S_2, S_3, D_6 devices, which forms a large commutation loop with a large stray inductance. And the NPC I-type 3-level scheme based on the IHV package uses 6 modules to form a phase of the bridge arm, the modules are connected by laminated busbars, as is shown in Figure 8(c), the actual large commutation circuit needs to pass through the module and the corresponding laminated busbar, further increasing stray inductance. According to the system measurement, it is generally up to 200nH, much larger than the module recommended 30nH, making the turn-off overvoltage abnormally high, and the module will fail easily due to overvoltage.

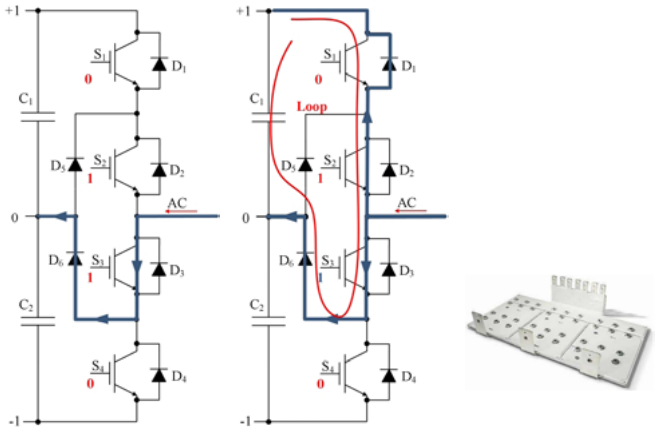


Figure 8

Especially in some applications, the volume requirement is higher, part of the occasions can not add absorption capacitor, so the traditional analogue drivers can only rely on the active clamping function. Based on the active clamping technology, the actual application of the clamping effect is affected by bus fluctuation, temperature and other factors, and due to the large stray, the active clamping often acts under some of the normal operating condition, resulting in the clamp diode a risk of failure, which brings hidden dangers to the reliable operation of the IGBT.

Large switching delay for high voltage IGBT modules

IHV package IGBT used in 3300V inverter belongs to the high-end module in the industrial field of semiconductor modules, the market can supply relatively few products. In the face of growing demand for equipment, the supply will fall short of demand. Due to the different technical routes of various module manufacturers, some manufacturers of IGBT exist switching delay problem, such as the turn-off delay of 4500V/1200A module of A manufacturer is about 7us, as is shown in Figure 9, while some of the controller's

dead time setting requirements are <4us, which brings a great challenge to the controller's dead time setting.

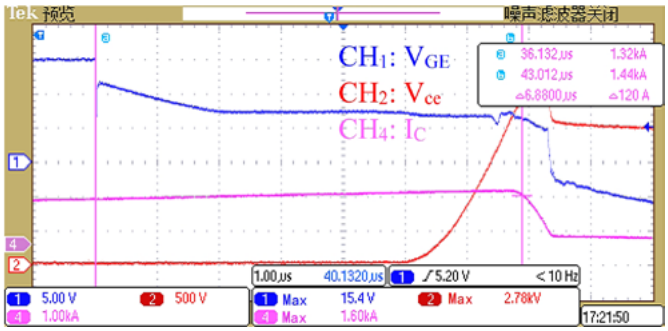


Figure 9: Tdoff time of the module of A manufacturer tested at VDC=2000V, IC=1500A

Demand of IGBT intelligence maintenance

Compared with the traditional 2-level, there are 12 IGBTs in the 3-level inverter, which is twice as the 2-level, and each IGBT has at least two types of faults: undervoltage and short-circuit, which makes a total of 24 types of faults. The traditional analog gate driver can't distinguish between undervoltage or short-circuit faults, which leads to a big challenge in analyzing the whole machine when problems occur in the actual R&D and debugging or in the field, because only the IGBT faults are reported, not including the type of faults. At present, the IGBT gate drivers of 3300V inverter of most manufacturers are standard analogue gate drivers of PI, there is no protection measures for IGBT failure after-sales maintenance of inverter, which can not meet the equipment manufacturers' demand of targeting the maintenance market through intelligent technical means.

Key technologies of intelligent IGBT gate driver

In response to the problems above in the application of high voltage IGBT in 3300V coal mine inverters, Firstack has developed a new generation of plug-and-play intelligent IGBT gate drivers: the HV1027P. Compared with traditional analogue gate drivers, there are the following features through digital innovation.

Fast short-circuit detection based on di/dt

As is the timing control of the inner and outer IGBT shown earlier, especially in the short-circuit state, the earlier the short-circuit protection is performed, the safer the inner and outer IGBT of the NPC I-type 3-level are. The intelligent gate driver uses a fast short-circuit detection technology based on di/dt, the basic principle of which is shown in Figure 10 (a). Inside the module package, there is an equivalent stray inductance L_{PE} in the power E terminal and auxiliary E terminal, which is generally around 5-10nH, and the change di/dt of the current flowing through the IGBT will produce a voltage drop V on the L_{PE}, which is calculated by:

$$V = L_{PE} \times di/dt \qquad (3\text{-}1)$$

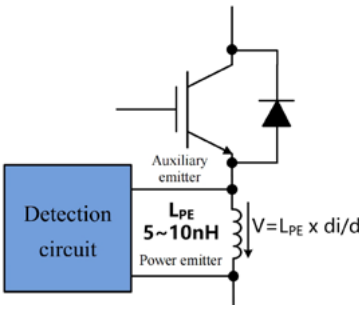


Figure 10: di/dt detection principle diagram Intelligent gate driver with di/dt detection

Since the di/dt of the current under normal condition is generally at 10A/us, while the di/dt under short-circuit condition is at 1000kA/us, the voltage drop difference produced is very large, and the gate driver will be able to quickly determine whether short-circuit protection occurs and provide effective protection by detecting the voltage drop V. As is shown in Figure 10(b), the gate driver has added a reed mounted on the power E terminal of the module for the di/dt protection detection function.

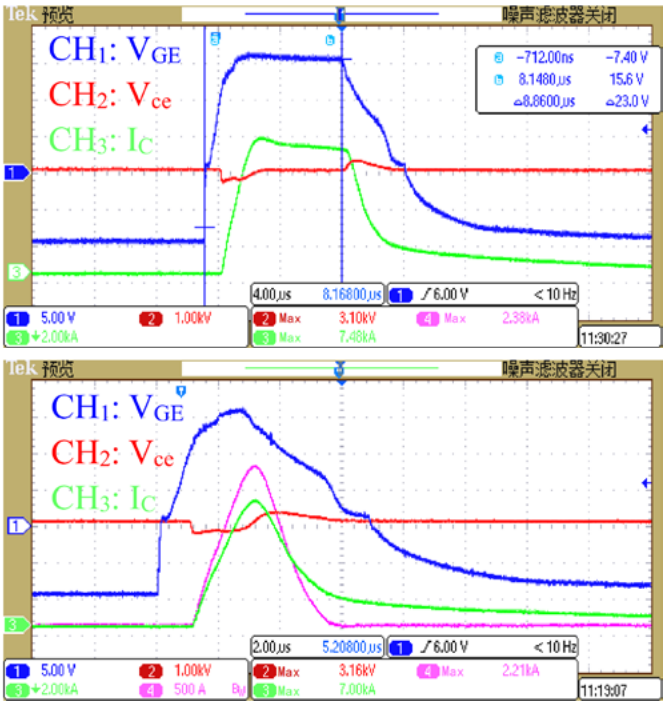


Figure 11: Top: Based on Vce short-circuit detection
Bottom: Based on di/dt short-circuit detection

As is shown in Figure 11, the short-circuit protection process based on Vce detection and di/dt detection are given respectively. From the test waveform, the protection time based on Vce short-circuit detection is 8.9us, and the protection time based on di/dt short-circuit detection is 2.7us, which is reduced by nearly 70%. In the timing coordination of high voltage module NPC I-type 3-level short-circuit fault protection, the inner IGBT module withstands the shorter short-circuit time, which is safer.

Digitally dynamic advanced active clamping D^2A^2C technology

As is the timing control of the inner and outer IGBT described, especially the timing control in the short-circuit state, if there is a wrong timing, such as the inner IGBT turned off first, will lead to IGBT overvoltage, which requires the active clamping circuit clamps the voltage at both terminals of the IGBT when the inner IGBT is turned off, so the precision of the clamp voltage of the active clamp circuit as well as the reliability of the clamp circuit itself is critical. In order to solve the inherent defects of the basic active clamping, and improve the problems of DA^2C[2] oscillation and TVS power consumption, Firstack innovatively put forward the digitally dynamic advanced active clamping D^2A^2C technology. As is shown in Figure 12(a), the CLPD processor samples the TVS breakdown current via the CS circuit, and controls a digitally controlled current source connected to the gate of the IGBT. When the TVS breakdown current is larger than the set threshold, the CPLD push-pull circuit will turn off the -15V power supply to remove the low-resistance path. According to the breakdown current size, control the size of the digitally controlled current source, so as to regulate the gate voltage as well as the TVS current. The technique can effectively control the current flowing through the TVS, so the clamping voltage is more accurate. The following Figure 12(b) is the short-circuit test waveform of intelligent gate driver products based on Infineon FF1000R17IP4 module. The turn-off moment Vce voltage is basically clamped at 1380V, and the turn-off process is very smooth with no violent oscillation.

Meanwhile, the TVS loss of D^2A^2C[3] and DA^2C are further compared on the platform, the specific test data are given in Figure 13, which gives the change of the TVS breakdown loss with the size of turn-off current. It can be seen that when the TVS breakdown current is large, the TVS loss of D^2A^2C is only 1/3 that of the DA^2C, and with the turn-off current becomes larger, the loss is basically unchanged, which greatly improves the life and reliability of the active clamping circuit.

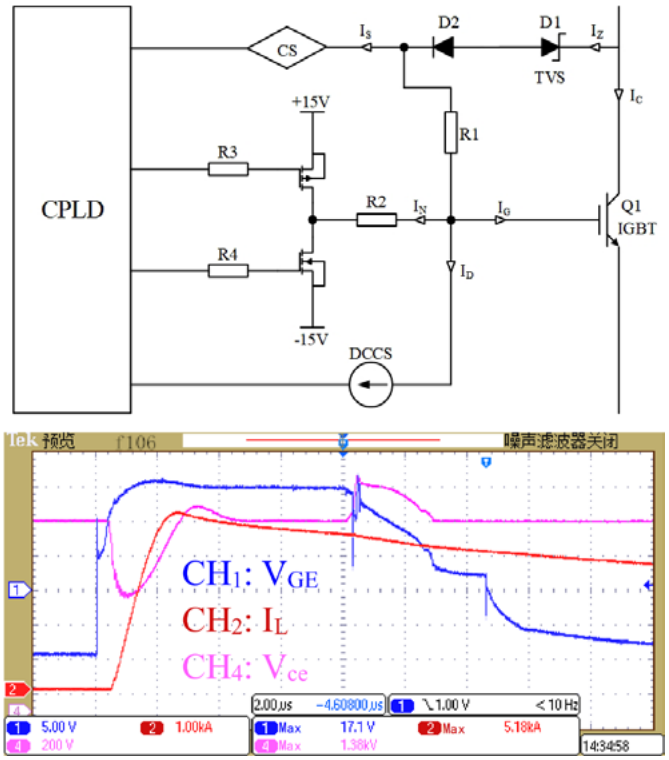


Figure 12:
Top: Digitally dynamic advanced active clamping
Bottom: Test waveform under short-circuit condition

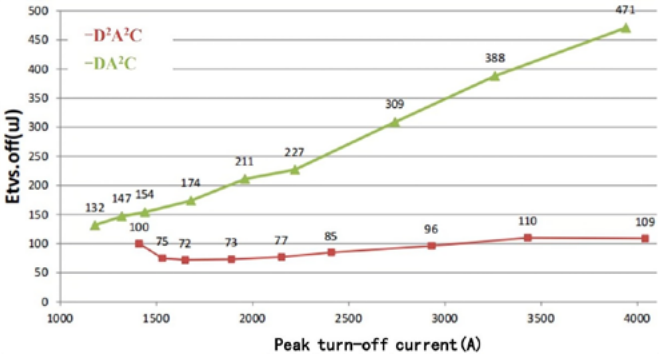


Figure 13: Comparison of the TVS power consumption

Multi-level turn-off technology

The effect of the gate resistor on the turn-off characteristics of the IGBT is that the larger the Rg is, the smaller the turn-off overvoltage is. In order to solve the problem of the inner IGBT turn-off overvoltage, a better idea is to increase the turn-off resistor. However, the increase of Rg will bring about the increase of turn-off delay and turn-off loss, which affects the dead time setting and thermal design of the whole machine.

Multi-level turn-off technology makes use of the influence mechanism of the turn-off resistor on the turn-off characteristics of the IGBT, the basic principle is to divide the turn-off process of the IGBT into three levels. Different from the traditional single turn-off resistor value, there are three different values of turn-off resistor at different times during the turn-off process, as is shown in Figure 14, MCU in the digital gate driver is in the control of the specific moment that R_1, R_2, R_3 are put into the gate circuit.

Based on the three-level turn-off process, three resistors are optimized to achieve effective suppression of voltage spikes, and to optimize switching delay as well as switching loss, to meet the needs of different applications of IGBT.

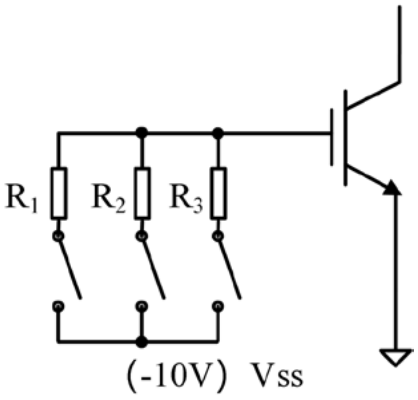


Figure 14: Multi-level turn-off resistor diagram

Turn-off voltage spike suppression

In order to test and verify the effect of multi-level turn-off technology, the corresponding comparison test was carried out. Figure 15 shows the voltage overvoltage V_{CE_MAX} of the test inner IGBT S_3 with and without multi-level turn-off technology, and the waveforms are shown as follows.

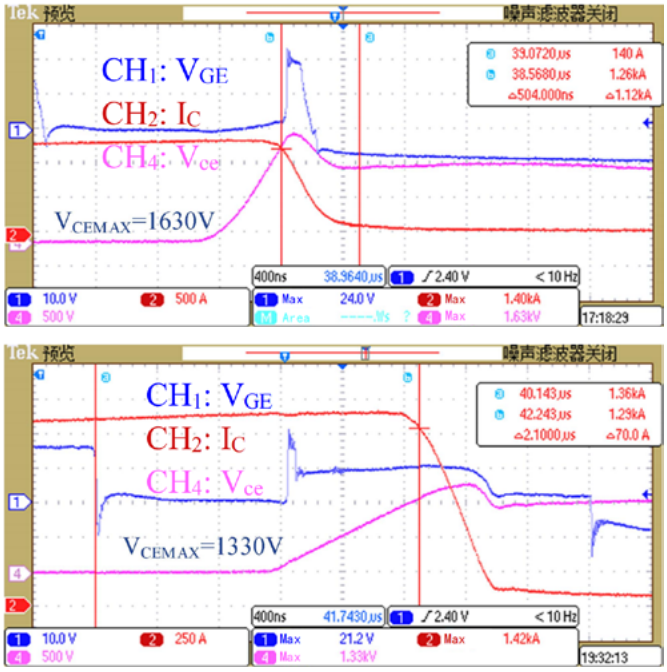


Figure 15:
Top: Test waveform without multi-level turn-off
Bottom: Test waveform with multi-level turn-off

From the comparison test results, under the same experimental condition, V_{CE_MAX} without multi-level turn-off = 1630V and V_{CE_MAX} with multi-level turn-off = 1330V, the voltage overvoltage

decreased by nearly 20%. Through reasonable parameter configuration, even if the circuit stray inductance reaches 200nH, it can be effectively suppressed. The technology is especially suitable for applications, which can eliminate the absorption capacitor and further reduce the size of the inverter.

Switching delay optimization

In order to verify the effect of optimizing the delay, the corresponding comparison test was carried out. Figure 16 is the test with and without multi-level turn-off delay Tdoff, the waveforms are shown below.

From the comparison test results, under the same experimental condition, Tdoff without multi-level turn-off = 6.9us and Tdoff with multi-level turn-off = 4.8us, with a nearly 30% decrease in delay time. The dead time setting can be greatly reduced, the application range of the IGBT module is expanded, and the quality of the output waveform on the inverter side is improved.

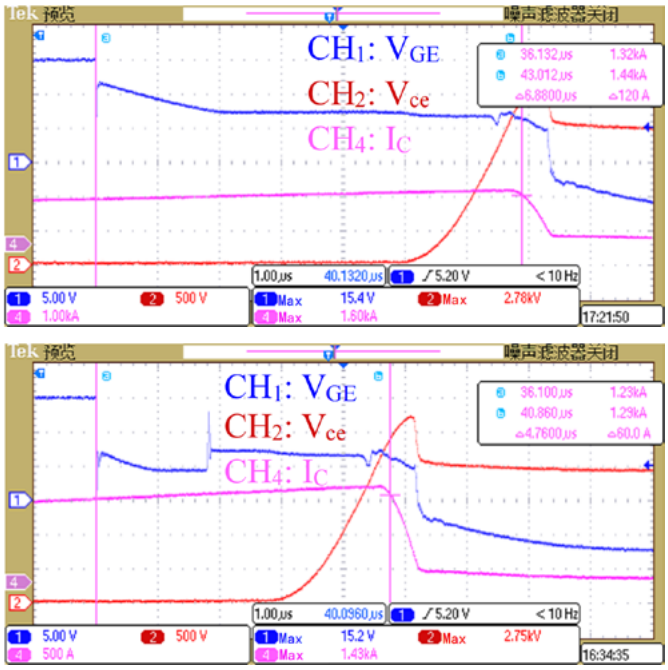


Figure 16:
Top: Test waveform without multi-level turn-off
Bottom: Test waveform with multi-level turn-off

Intelligent fault communication

The traditional analogue gate driver aggregates undervoltage faults and short-circuit faults to Fault port, and when Fault port signal is low level, the master computer determines that there is a gate driver fault, but it cannot distinguish whether it is an undervoltage fault or a short-circuit fault. It is also impossible to interact with the master computer for more information. Intelligent fault communication technology is based on the MCU in the digital gate driver, multiplexing Fault port, through the encoding of fault information transmission of the serial communication method, as is shown in Figure 17, the master computer can be informed of the fault type and the order of the fault occurrence. Through the distinction between the type of faults can be carried out to assist in the rapid positioning of the entire machine faults. At the same time, the communication port can be customized with the master computer encryption protocol, and target the maintenance market.

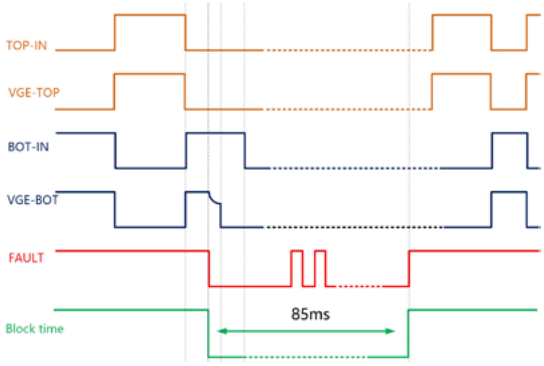


Figure 17: Intelligent fault communication

Conclusion

3300Vac inverter is increasingly in demand in the coal mining industry. As the core of high voltage and high power electronic equipment, IGBT and gate driver play an important role. Conventional analogue gate drivers cannot meet the demand for high reliability, miniaturization and intelligence.

Firstack has developed a new generation of digital IGBT gate driver, developed di/dt fast short-circuit detection, multi-level turn-off, intelligent fault communication technology, which can better solve the timing problems of inner and outer IGBT in 3300Vac coal mine inverters, too large turn-off voltage spike of the inner IGBT, large delay the of the high voltage IGBT module, and maintenance of intelligent needs, which meets the system for reliability, miniaturization and intelligence demand.

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[3] Firstack Technical documentation: HV1027P.pdf

www.firstack.com

Adding USB Type-C with USB Power Delivery to Battery-powered Applications

A USB Type-C® port with USB Power Delivery (PD) is becoming the standard port for charging single- and multi-cell battery-powered devices. Applications such as wireless speakers, power banks and power tools have been transitioning from proprietary charging ports, legacy USB ports and barrel-jack ports to a standardized USB PD port. USB PD offers a universal alternative for fast and convenient charging, removing the need for users to carry around several adapters or cables with them – helping design engineers create smaller applications with faster charging and fewer components.

By Eric Beljaars - Business Lead, USB Type-C and PD controllers, Texas Instruments

As these applications become more feature-rich, compact and power-hungry, it becomes necessary to deliver more power in a smaller solution size. Concurrently, consumers are beginning to expect USB Type-C on their new devices. But implementing a USB PD port has historically been quite challenging for product developers.

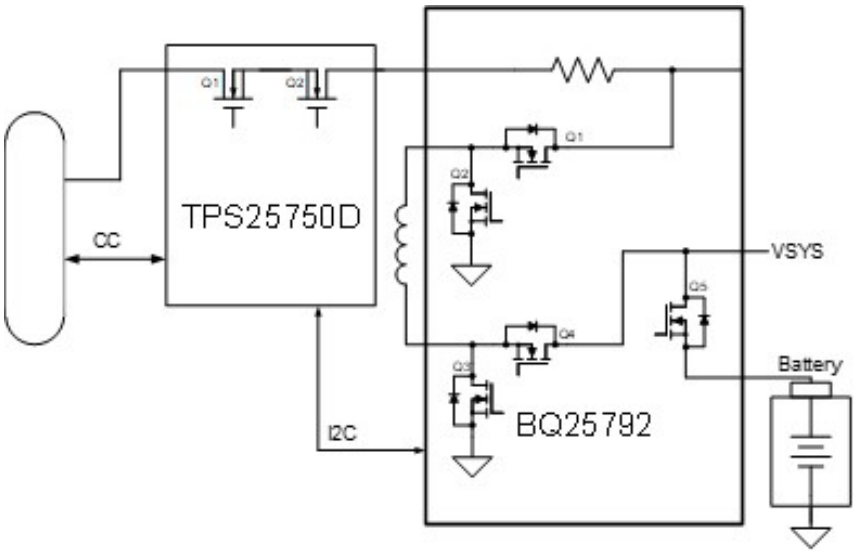

Figure 1: TPS25750D and BQ25792 USB PD Battery-charger Implementation

Simplifying your design challenge

In the past, adding a USB PD port required a very in-depth understanding of USB specifications and a large firmware and hardware development effort. Several different components need to work together in order to facilitate USB PD support. The two main integrated circuits (ICs) required to complete a USB PD port for charging applications are the USB PD controller IC and battery-charger IC. These ICs typically operate independently of one another and cannot work in a system without a lot of involvement from an external Microcontroller (MCU).

This limitation also then requires MCU firmware development in order to communicate events happening on the USB PD port to the battery-charger IC. For example, once the USB PD controller IC negotiates a new voltage and current on the USB Type-C port (or a new power contract), the microcontroller needs to read this information back from the USB PD controller and then update the battery chargers' charge current and charge voltage based on what's connected to the USB PD port. Additionally, sourcing power out of the USB PD port to charge external devices requires additional communication between the USB PD controller, MCU and battery charger.

Programming the MCU to interface between the USB PD controller and battery charger is usually not the only firmware development required when adding USB PD. Typical PD controller ICs require some form of firmware development to configure the PD controller behavior itself, such as compiling some code or scripting functions together. Configuring the USB PD controller is necessary in order to ensure that the settings on the PD controller meet your system requirements, including which voltages and currents the system can sink and which ones it can source.

Designing with TI controllers and chargers

To help simplify the design of a USB PD port for battery-powered applications up to 45 W, the TPS25750 USB PD controller adds I2C host support to directly control the BQ25792 bat-

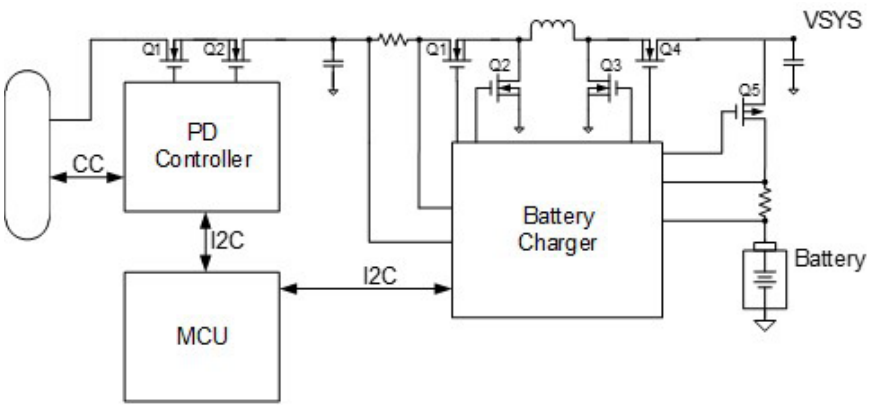

Figure 2: MCU-based Nonintegrated Solution

	USB PD battery-charger implementation up to 45 W	MCU-based nonintegrated USB PD battery-charger implementation
External MCU	Not required; the TPS25750 is the I^2C host controller for the battery charger	Required; the USB PD controller and battery charger operate independently
Firmware development	Not required; the system is configurable through a Q&A GUI	Required; necessary to interface with the USB PD controller and battery charger through the MCU
System power paths	All system power paths are integrated in the USB PD controller and battery charger	External FETs are necessary to complete the solution
Solution size	Approximately 55 mm^2	Approximately 150 mm^2

Table 1: Integrated vs. non-integrated USB PD battery-charger implementation comparison

tery charger without any intervention from an external MCU. The TPS25750 USB PD controller will automatically update the charging parameters of the BQ25792 over I2C based on the power negotiation over the USB PD port. Thus, the external MCU is now unnecessary, and you don't need to develop firmware to add a USB PD port to battery-powered applications.

Configuring USB PD port behavior with the TPS25750's web-based graphical user interface (GUI) entails answering a few multiple-choice questions about what your USB PD port needs to support – no complex scripting, code compiling or firmware development is required. This doesn't just reduce bill-of-materials costs; it allows you to add USB PD without possessing in-depth expertise about the technology.

The TPS25750 and BQ25792 integrate all of the power paths required for the battery charger and USB PD controller. Figure 1 highlights how these devices simplify the implementation of a USB PD port for battery-powered systems up to 45 W. When using these two ICs together, the USB PD port will be able to support bidirectional power to both source and sink power, thus enabling the system to charge or be charged from the USB PD port when attached to an external device like a laptop, smartphone, headphones or AC adapter.

In addition to these system implementation benefits, the TPS25750D and BQ25792 integrate all of the system's field-effect transistors (FETs) and remove the need for an external MCU, enabling you to achieve a very small solution size. When compared to an MCU-based nonintegrated USB PD battery-charging implementation, the typical system solution size is around 150 mm^2. When using the TPS2570 and BQ25792, it is possible to achieve a system solution size around 55 mm^2.

Table 1 compares USB PD charging for integrated and nonintegrated MCU-based solutions.

The trend toward using USB PD for charging has recently become more urgent, with regulations pushing for universal chargers. Updating your system to charge from USB PD is now easier than ever with the TPS25750 and BQ25792, enabling you to move to the latest universal charging connector while not compromising on solution size.

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Transformer-Based Voltage Regulators with Flexible TLVR Structure for Fast Dynamic Response

An extremely fast dynamic response is highly desirable in voltage regulators (VRs) for various applications requiring high current up to thousands of amperes. This article presents transformer-based VRs with a trans-inductor voltage regulator (TLVR) structure designed to achieve an extremely fast response during load transients. Overcoming the drawbacks of traditional TLVR structure, transformer-based VRs with TLVR structure feature great design flexibility and extremely fast transient response, which results in smaller output capacitance and solution size, and lower system cost. Detailed experimental results and a case study are provided to demonstrate the comprehensive benefits of transformer-based VRs with TLVR structure.

By Xingxuan Huang, Senior Applications Engineer, Xinyu Liang, Senior Manager, Product Applications, and Chuan Shi, Staff Applications Engineer, Analog Devices

Introduction

Nowadays multiphase VRs play an increasingly important role as they are used to power a wide range of microprocessors, such as CPUs, GPUs, and ASICs. In recent years, the power demand for these microprocessors has been increasing drastically, especially in telecom and some emerging applications, such as crypto mining and autonomous driving systems. Microprocessors are thereby requiring higher current with a higher slew rate. Hence, VRs are required to have a faster dynamic response during load transients to satisfy the output voltage ripple requirements. From the perspective of system size, an extremely fast dynamic response is highly attractive to reduce the required output capacitance and shrink the size of output capacitors. Moreover, smaller output capacitance and fewer output capacitors benefit the system cost. This article will present a transformer-based VR solution with a TLVR structure designed to realize extremely fast load transient response and substantially shrink the size and cost of output capacitors. When introducing TLVR structure in transformer-based VR solutions, traditional challenges of TLVR structure can be easily tackled.

Design and implementation details will be provided, and comprehensive benefits will be demonstrated with a case study based on practical applications. It also should be noted that the design and implementation details in this article are currently patent pending.

TLVR structure is an effective implementation to accelerate dynamic response during the load transients of multiphase VRs.[1,2,3] As shown in Figure 1, the TLVR structure leverages TLVR inductors to replace the output inductors in traditional multiphase VRs. A TLVR inductor can be regarded as a 1:1 transformer that possesses a primary winding and a secondary winding. The coupling of all TLVR inductors is realized by connecting the secondary windings of all TLVR inductors. The current in the secondary side of TLVR inductors, I_{LC}, is determined by the control signals of all different phases. Because of the coupling effect, the output current of all phases can ramp up or down at the same time once the duty cycle of one phase of the VR changes to respond to the load transient. That is why the TLVR structure can achieve excellent load transient performance.

Transformer-Based VRs

Transformer-based VRs have been competitive power solutions for various microprocessors. Equipped with a step-down transformer, transformer-based VRs feature a high and flexible step-down ratio, a simple and compact structure, and high efficiency. Compared to transformerless multiphase VRs, transformer-based VRs allow much higher input voltage and hence open a whole new world for simplifying VR design and achieving higher efficiency.

Figure 2 shows the circuit diagram of one representative example of the transformer-based VR. The VR circuit features a step-down transformer with two secondary windings and a current doubler structure on the secondary side. More secondary

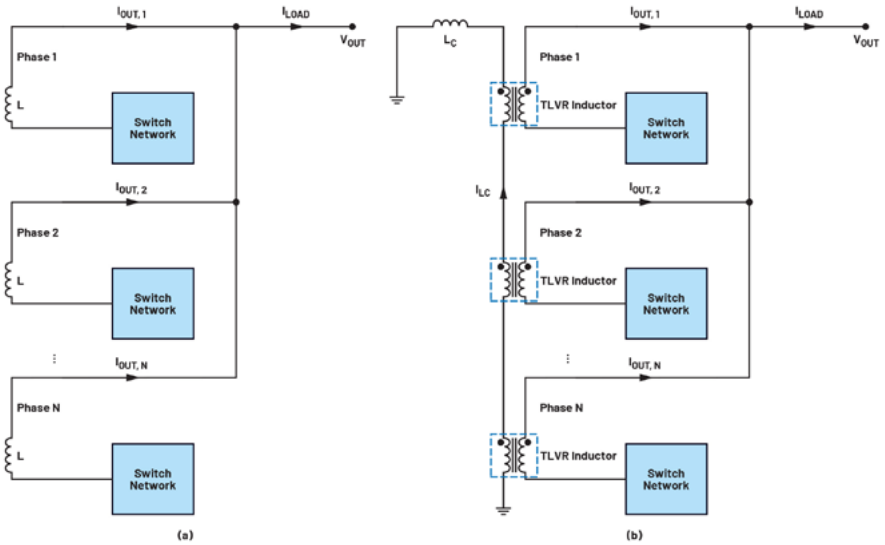

Figure 1: (a) A circuit diagram of a traditional multiphase VR without TLVR structure and (b) a circuit diagram of a multiphase VR with TLVR structure.

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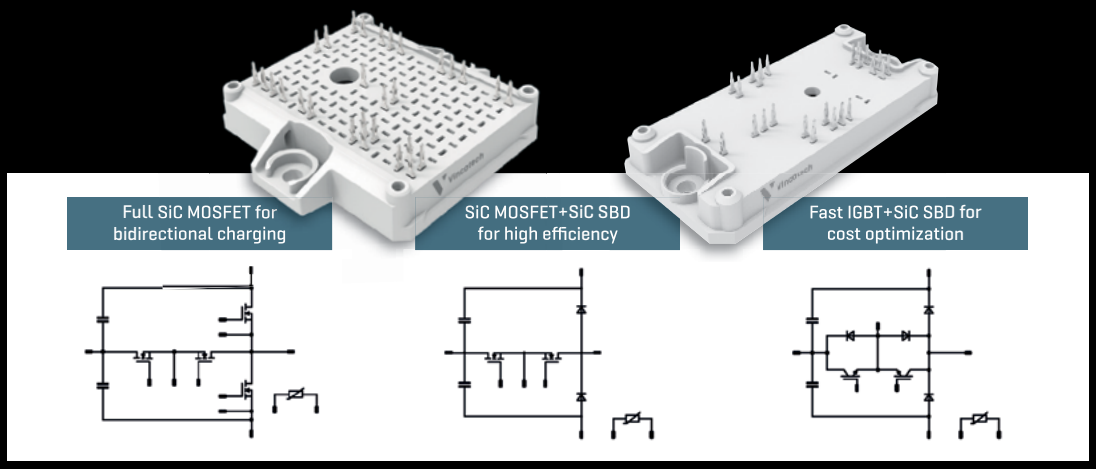

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windings can be designed to achieve higher output current and power density, and no additional control signals are needed on the secondary side. With proper control circuits and strategy, multiple example VR circuits in Figure 2 can be easily connected in parallel to provide the required current for a wide range of high performance microprocessors. Therefore, the VR circuit shown in Figure 2 is used as an example throughout this article.

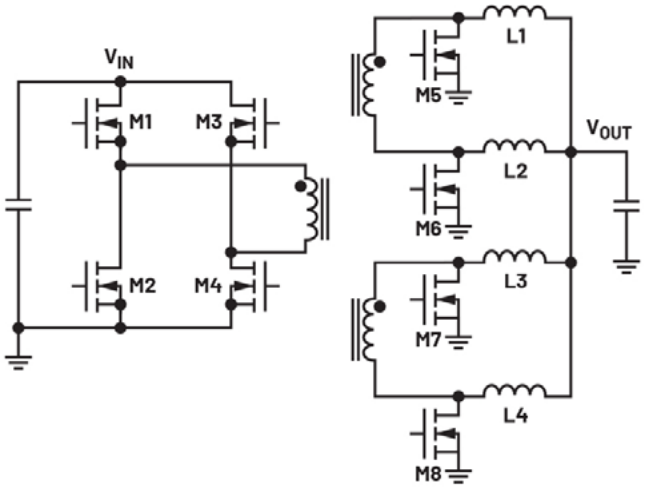

Figure 2: A circuit diagram of one transformer-based VR example.

Benefits of TLVR Structure in Transformer-Based VRs

It is well demonstrated that the TLVR structure can significantly accelerate the dynamic response of the VRs without any step-down transformer during load transients. However, such superior dynamic performance is introduced together with numerous challenges.[1,2,3] Without any step-down transformer, these transformerless VRs typically operate with low duty cycle and high voltage applied in both the primary and secondary sides of TLVR inductors. The high voltage-second in the secondary side of TLVR inductors results in a high circulating current in the secondary side of TLVR inductors and additional power loss during the steady state operation. Hence, as can be seen in Figure 1b, an additional inductor L_c should be added to limit the circulating current in the secondary windings of TLVR inductors.[1] The additional inductor further increases the system loss and cost.

The challenges brought by the TLVR structure can be smoothly tackled when introducing the TLVR structure in transformer-based VRs. By combining the TLVR structure with the step-down transformer, the drawbacks of the TLVR structure become much less significant due to the high step-down ratio of the main transformer. Meanwhile, the extremely fast dynamic response can still be achieved, as the coupling effect pushes the current of all phases to respond simultaneously during load transients. Because of the step-down transformer, the voltage applied to the TLVR inductors becomes much lower, leading to lower inductor loss. The inductance of the additional inductor required in the secondary side of the TLVR inductors can be much lower. In fact, by leveraging the parasitic inductance, the additional inductor can be eliminated, as well as the additional loss and cost brought by the inductor. In addition, the insulation issue associated with the TLVR inductors and the additional inductor is no longer a concern.

Transformer-Based VRs with Flexible TLVR Structure

In transformer-based VRs with TLVR structure, all output inductors in the circuit are replaced by the TLVR inductors. Moreover, two types of implementations can be realized when applying the TLVR structure in transformer-based VRs, which offers great flexibility when implementing this structure. Figure 3 shows the circuit diagrams of the two types of implementations using the example of two VR modules shown in Figure 2 connected in parallel. The implementation in Figure 3a is called series connection since all the secondary windings of TLVR inductors are connected in series. The other implementation shown in Figure 3b is called a series-parallel connection. In Module 1, the secondary windings of L11 and L12 are connected in series before they are connected in parallel with the series connection of the secondary windings of L13 and L14. Such a connection of secondary windings of TLVR inductors in Module 1 is finally connected in series with the counterpart connection in Module 2, as shown in Figure 3b. Similarly, two implementations with TLVR structures in Figure 3 can be realized when more than two transformer-based VR modules are connected in parallel.

Enhanced flexibility in design and implementation does not increase the control complexity. The same control scheme is applied for the two implementations of the transformer-based VR with TLVR structure. Here, the control scheme for the transformer-based VR with three modules in parallel is introduced as an example. Phase shift is inserted between control signals for different VR modules. The inserted phase shift between Module 1 and Module 2 is 60°, and a phase shift of 60° is inserted between control signals for Module 2 and Module 3. If there are N modules in parallel, the inserted phase shift between two adjacent modules is 180°/N.

Based on the proposed control scheme, the voltage applied to all TLVR inductors can be derived. Figure 4 summarizes the voltage waveforms of all TLVR inductors in the transformer-based VR with two modules connected in parallel. Since the two types of implementations in Figure 3 have the same control signal, the inductor voltage waveforms are also the same. It can also be observed that L11 and L13 have the same voltage waveform, which is the case for L12 and L14 as well. These inductor voltage waveforms effectively explain why the series-parallel connection in Figure 3b is legitimate. The current in the secondary side of TLVR inductors, I_{sec}, has a high frequency ripple at 4× switching frequency of MOSFETs in the primary side of the main step-down transformer. With N (N > 2) modules connected in parallel, the current ripple of I_{sec} will be at a higher frequency (2N × the switch-ing frequency), and the magnitude of I_{sec} can be further reduced. Therefore, the proposed control scheme with phase shift can not only reduce the output voltage ripple, but also effectively suppress the ripple of I_{sec}, and hence the conduction loss in the secondary side of TLVR inductors.

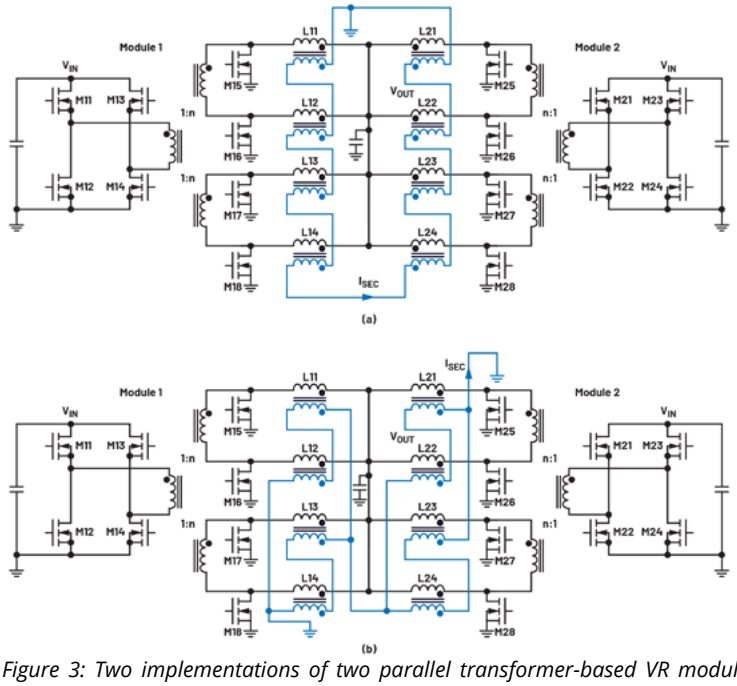

Figure 3: Two implementations of two parallel transformer-based VR modules with TLVR structure: (a) a series connection and (b) a series-parallel connection.

Also, no additional inductor is required in the transformer-based VR with TLVR structure. The additional cost and loss brought by the additional inductor are eliminated as well, which substantially benefits the system's efficiency and cost. Because of the high transformer step-down ratio (small n), the voltage of TLVR inductors is reduced substantially compared to the transformerless VR with TLVR structure. Hence, it is not necessary to introduce the additional compensation inductor Lc in the secondary side of the TLVR inductor to suppress the current ripple. Detailed information about the TLVR inductor voltage can be seen in Figure 4. In this case, the parasitic inductance in the circuit and the leakage inductance of TLVR inductors play a critical role in shaping the current in the secondary side of TLVR inductors, I_{sec}. To further improve the dynamic performance during the load transient, it is important to reduce the leakage inductance and the parasitic inductance in the secondary side of TLVR inductors.

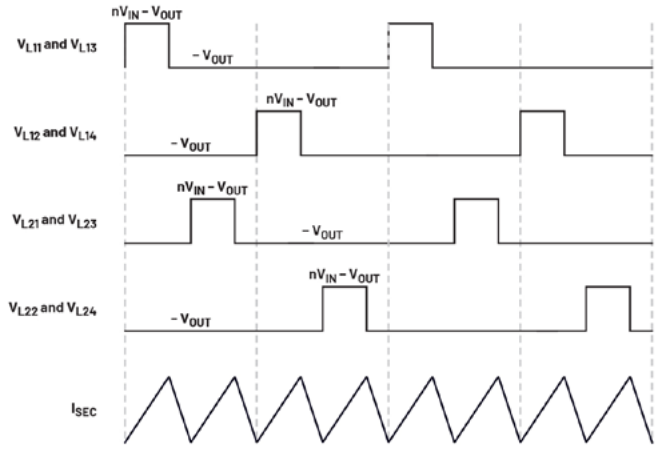

Figure 4: Waveforms of voltage and secondary current of TLVR inductors in transformer-based VR modules with TLVR structure (two modules in parallel).

Prototypes and Experimental Results

Both implementations of the transformer-based VR module with TLVR structure are designed and built, including the series connection version and the series-parallel connection version. Figure 5a displays the 3D model of a typical TLVR inductor. The built module prototype can be seen in Figure 5b. Both versions have the same size as their counterpart without TLVR structure. In other words, adopting TLVR inductors to realize the TLVR structure does not increase the VR module size, no matter whether a series connection or series-parallel connection is implemented.

The extremely fast load transient performance of the transformer-based VR with TLVR structure has been successfully demonstrated with the built prototypes. The experimental setup consists of two VR modules operating in parallel, as shown in Figure 5b. No additional inductor is installed in the secondary side of TLVR inductors. The load transient is between 20 A and 170 A with a slew rate of 125 A/µs. The excellent load transient response of the transformer-based VR with TLVR structure is clearly illustrated in the baseline comparison shown in Figure 6, in which the series-parallel connection version is used as an example. To make a fair comparison, the case without the TLVR structure is realized by disconnecting the connection in the secondary side of TLVR inductors. As the load current steps up from 20 A to 170 A, the transformer-based VR with TLVR structure can regulate the output voltage more quickly with a much lower peak-to-peak voltage ripple.

An extremely fast load transient response is achieved in the transformer-based VR with TLVR structure, after conducting further improvement. Detailed transient waveforms can be seen in Figure 7. Under the same transient from 20 A to 170 A, the peak-to-peak output voltage ripple is only 23.7 mV, thanks to the extremely fast re-

sponse brought by the TLVR structure. Adopting the TLVR structure substantially accelerates the dynamic response and hence reduces the peak-to-peak output voltage ripple by 62%. The measured high control bandwidth of 115 kHz also demonstrated the extremely fast load transient response enabled by the TLVR structure. A detailed comparison is summarized in Table 1.

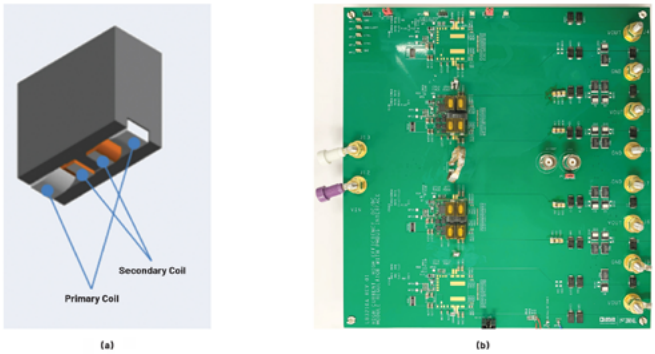

Figure 5: (a) A 3D model of TLVR inductor and (b) two transformer-based VR prototypes with TLVR structure in parallel on a demo board.

Structure	With TLVR Structure	Without TLVR Structure
Output Capacitance	15.2 mF	15.2 mF
Voltage Ripple (pk-pk)	23.7 mV	62 mV
Control Bandwidth	115 kHz	45 kHz
Phase Margin	69°	40.7°

Table 1: Comparison of Dynamic Response Between a Transformer-Based VR with TLVR Structure and Without TLVR Structure.

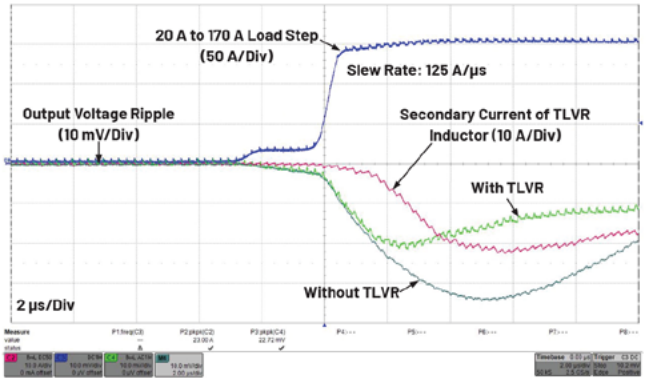

Figure 6: Comparison of load transient response of a transformer-based VR with TLVR structure and without TLVR structure.

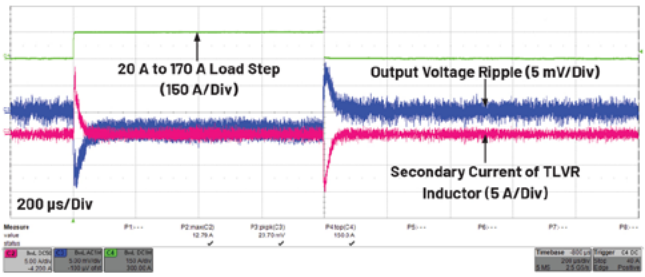

Figure 7: Extremely fast load transient response of a transformer-based VR with TLVR structure.

Case Study

To further showcase the benefits of combining transformer-based VRs with the TLVR structure, this section introduces a case study of transformer-based VR based on specifications from practical applications. Both transformer-based VR solutions with and without TLVR structures are implemented and tested to provide a 0.825 V/540 A rail. Details of specifications and test results are summarized in Table 2. With comparable phase margin and gain margin, the transformer-based VR solution with TLVR structure achieves 61% higher control bandwidth than the VR solution without TLVR structure. Thus, the extremely fast transient enabled by the TLVR structure is demonstrated again, as shown in Figure 8. The peak-to-peak output voltage ripple is only 40.92 mV, lower than 5% of the 0.825 V output voltage.

With 39% output capacitance saved, the VR solution with the TLVR structure still realizes a much lower peak-to-peak voltage ripple compared to the VR solution without the TLVR structure. Thus, the number of output capacitors is reduced by 27%, resulting in a tremendous decrease in system solution size. Also, the cost of output capacitors can be cut by 43%, thanks to the extremely fast transient response enabled by the TLVR structure.

Generally, transformer-based VR with TLVR structure featuring extremely fast dynamic response can effectively reduce the output capacitance, while still maintaining low output voltage ripple during fast load transients. In addition, no additional inductor is required in transformer-based VRs with TLVR structure. Therefore, transformer-based VR solutions with TLVR structure can not only significantly reduce the total solution size but also result in a substantial reduction in solution cost, especially the cost of output capacitors. Two implementations available for use further bring the benefit of great flexibility, and meanwhile the control complexity is not increased.

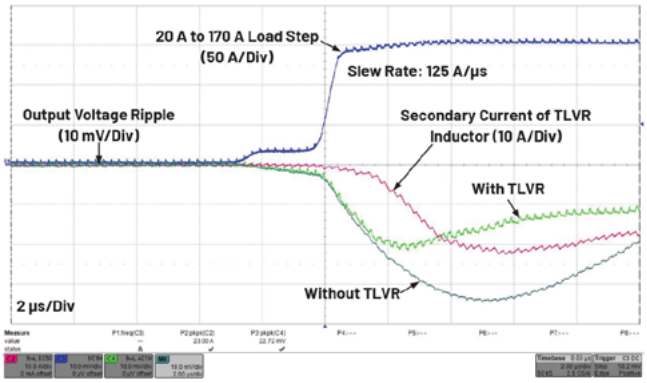

Figure 8: An extremely fast load transient response of a transformer-based VR with TLVR structure under 150 A to 350 A load transient (three VR modules in parallel).

Structure	VR Solution with TLVR Structure	VR Solution Without TLVR Structure
Output Current	540 A	540 A
Output Voltage	0.825 V	0.825 V
Number of VR Modules	Three in parallel	Three in parallel
Switching Frequency	550 kHz	550 kHz
Voltage Ripple (pk-pk)	40.92 mV	61.15 mV
Control Bandwidth	55 kHz	34.2 kHz
Phase Margin/ Gain Margin	78.8°/9.9 dB	65.5°/10.4 dB
Total Output Capacitance	24.88 mF	40.92 mF
Number of Output Capacitors	74	101
Cost of Output Capacitors	$9.50	$16.75

Table 2: A Case Study of Transformer-Based VR Solution Based on Specifications from a Customer.

Summary
VR solutions for microprocessors are required to have accelerated dynamic response as microprocessors consume higher current with a higher slew rate in a wide range of applications. This article introduces the transformer-based VRs with TLVR structure to achieve extremely fast dynamic response during load transients of microprocessors. By combining transformer-based VRs with TLVR structure, the traditional challenges of TLVR structure can be easily tackled because of the large step-down ratio of the main transformer. Excessive loss in TLVR inductors can be significantly reduced, and no additional compensation inductor is required, leading to lower loss and cost. Moreover, two types of implementations can be adopted when implementing TLVR structure in transformer-based VRs, which provides great flexibility in design and implementation. Both implementations can cover numerous VR modules in parallel with the same control scheme. The experimental results prove that both implementations can achieve extremely fast load transient response than their counterparts without TLVR structure, with 2.56× control bandwidth and 62% lower peak-to-peak voltage ripple. A detailed case study further presents the comprehensive benefits of transformer-based VRs with TLVR structure in solution size and cost.

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About the Authors

Xingxuan Huang is a senior applications engineer in Analog Devices CA, U.S.A., focusing on power products. He received his master's and Ph.D. degrees in electrical engineering from the University of Tennessee, Knoxville, in 2019 and 2021, respectively, with concentration on power electronics.

Xinyu Liang is the applications engineering manager in the Industrial and Multimarket Group at Analog Devices focusing on power products. He received his Ph.D. degree in electrical engineering in 2018 from North Carolina State University and he started his career at ADI in 2019 after graduation.

Chuan Shi is a staff applications engineer in Analog Devices CA, U.S.A. He received his Ph.D. degree in electrical engineering (with distinguished honor) from the University of Maryland, College Park, MD, U.S.A. His expertise is on modeling, analysis, design, and control of power electronic converters for automotive, industrial, and communication applications.

eFuses Feature Continuous Current up to 100 A

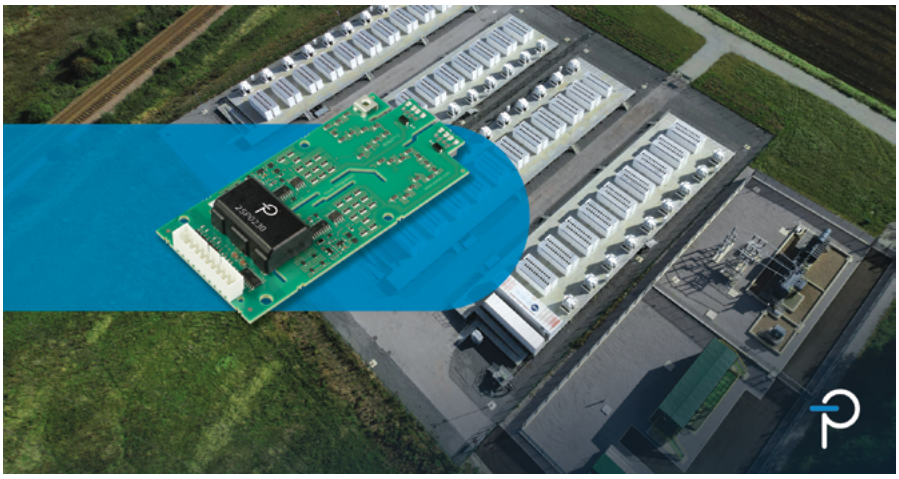
DigiKey announced that the EFUSE-48V100A reference design product from Vishay is now available for purchase globally from DigiKey. The Vishay eFuse features TrenchFET MOSFETs and is designed to handle continuous current up to 100 amps. It can operate continuously at maximum current with less than 14 watts of losses without requiring active cooling. The eFuse also features a pre-charge function, continuous current monitoring and overcurrent protection.

In addition to safely connecting and disconnecting to 48V power sources like high-energy battery packs, the EFUSE-48V100A also features fast disconnect of loads in under 2µs, a resettable fuse and an adjustable current limit. It is designed to work in battery management systems, EV test environments, solar installations, industry and home automation, industrial and server computing, networking, telecom and base station power supplies.

www.digikey.com

Gate Drivers for 62 mm SiC and IGBT Modules

Power Integrations announced a family of plug-and-play gate drivers for 62mm silicon-carbide (SiC) MOSFET and silicon IGBT modules rated up to 1700V, with enhanced protection features to ensure safe, reliable operation. SCALE™-2 2SP0230T2x0 dual-channel gate drivers deploy short-circuit protection in less than two microseconds, protecting the compact SiC MOSFETs against damaging over-currents. The drivers also include advanced active clamping (AAC) to protect the switches against overvoltage during turn-off, enabling higher DC link operating voltages.



Suited for applications such as railway auxiliary converters, offboard EV chargers and STATic synchronous COMpensator (STATCOM) voltage regulators for the power grid, 2SP0230T2x0 gate drivers are based on Power Integrations' proven SCALE-2 technology, resulting in higher levels of integration, smaller size, more functionality and enhanced system reliability. Power Integrations' compact 134 x 62mm 2SP0230T2x0 provides reinforced isolation at 1700V, enabling use for up to 1700V operation; this is 500V higher than conventional drivers, which are typically limited to 1200V.

www.power.com

GaN FETs Enable 75-231 Ampere Laser Diode Control in Nanoseconds for Lidar

EPC launches three laser driver boards dubbed EPC9179, EPC9181 and EPC9180 containing pulse current laser drivers of 75 A, 125 A, and 231 A, showcasing EPC's AEC-Q101-qualified GaN FETs. These FETs (EPC2252, EPC2204A, and EPC2218A) are 30% smaller and said to be more cost-effective than their predecessors. Designed for both long and short-range automotive lidar systems, these boards expedite solution evaluation with varied input and output options. All boards share identical functionality, differing only in peak current and pulse width. The EPC9179/81/80 boards are triggered from 3.3V logic or differential logic signals such as LVDS. For single-ended inputs, the boards can operate with input voltages down to 2.5V or 1.8V with a simple modification. EPC provides full schematics, BOM, PCB layout files and a quick start guide on its website.

www.epc-co.com

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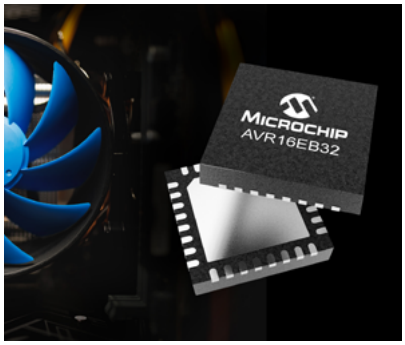
Microcontrollers Reduce Noise, Vibration and System Harshness in BLDC Applications



Microchip Technology has launched its AVR EB family of microcontrollers to offer a solution for addressing NVH and efficiency in a wide variety of cost-sensitive applications. AVR EB MCUs can adjust speed, timing and waveform shape - creating sinusoidal and trapezoidal waveforms - to improve the smoothness of motor operations, reduce noise and increase efficiency at high speeds. These adjustments can be made on the fly, with near-zero latency, using the AVR EB MCU's set of on-chip peripherals that enable multiple functions with minimal programming. The result is a reduction in code complexity, faster response to changes in operating conditions and lower overall Bill of Materials (BOM) cost since several tasks, such as reading environmental sensors and serial communication, can be performed independent of the CPU. Additionally, the devices' small form factor (as small as 3mm x 3mm) enables them to be mounted directly to the motor for a compact control solution.

www.microchip.com

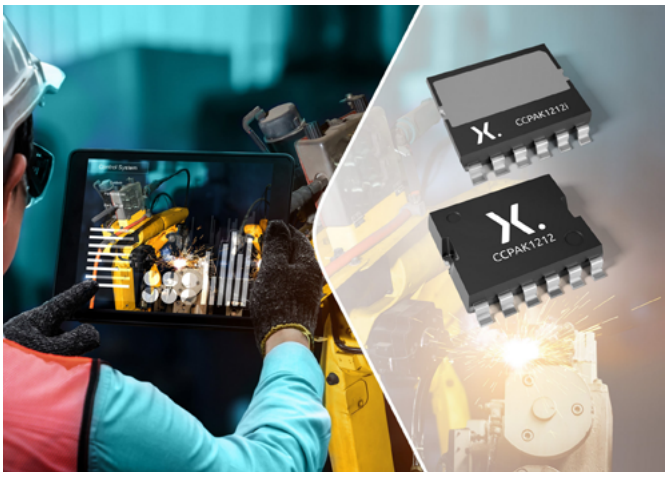
POWER2GO – Powerbank thought BIG

POWER2GO is basically a maxi version of a power bank offered by BMZ Group. It offers independence from the power grid, both in the event of a power failure and far away from the nearest power socket. Weighing 23kg and measuring 452 x 373 x 192mm, the portable energy storage unit offers a constant, long-term power output of 2,500W and can even operate devices with peak outputs of up to 5,700W without any problems. The energy density of the 2.5kWh power storage device is specified with 125Wh/kg and the protection class is according to IP 65, which certifies that the device is dust-proof and waterproof, and the fact that it does not require a fan and therefore operates absolutely quietly. The POWER2GO beats a conventional ICE-based generator not only in terms of size and weight. POWER2GO is quiet and emission-free.

https://power.bmz-group.com/en

GaN FETs in Compact SMD Packaging

Nexperia announced that its GaN FET devices, featuring high-voltage GaN HEMT technology in proprietary copper-clip CCPAK surface mount packaging, are now available to designers of industrial and renewable energy applications. Building on two decades of expertise in supplying high-volume, high-quality copper-clip SMD packaging, Nexperia is now proud to extend its packaging approach to GaN cascode switches in CCPAK. The GAN039-650NTB, a 33 mΩ (typ.) Gallium Nitride (GaN) FET within the CCPAK1212i top-side cooling package, ushers in a new era of wide bandgap semiconductors and copper-clip packaging. This technology is well-suited for renewable energy applications such as solar and residential heat pumps, further enhancing Nexperia's commitment to developing the latest component technology for sustainable applications. It is also suited to a wide spectrum of industrial applications such as servo drives, switched-mode power supplies (SMPS), server, and telecom.



Nexperia's CCPAK surface mount packaging uses Nexperia's proven innovative copper-clip package technology to replace internal bond wires. This reduces parasitic losses, optimizes electrical and thermal performance, and improves device reliability. For maximum flexibility in designs, these CCPAK GaN FETs are available in top- or bottom-cooled configurations to further improve heat dissipation.

The cascode configuration of the GAN039-650NTB enables it to deliver better switching and on-state performance, with a robust gate offering high margins against noise while eliminating the requirement for complex gate drivers and control circuitry; a standard silicon MOSFET driver is sufficient.

www.nexperia.com

650V Super Junction N-Channel MOSFETs

Central Semiconductor now offers several 650V Super Junction N-Channel MOSFETs designed for high-voltage, fast-switching applications. The latest additions, available in TO-220FP packaging, include the devices CDMSJ2204.7-650 (4.7A), CDMSJ2207.3-650 (7.3A), CDMSJ22010-650 (10A), CDMSJ22013.8-650 (13.8A) and CDMSJ22029-650 (29A). The Super Junction MOSFETs feature a die structure, which supports high-voltage with comparatively low on-resistance and fast switching speeds in applications like electric vehicle inverter, and solar.

www.centralsemi.com

Portfolio of Space-Screened GaN HEMTs

Teledyne e2v HiRel announces the addition of new space screened versions of its popular 100 V, 90 A and 650 V, 30 A high reliability gallium nitride high electron mobility transistors (GaN HEMTs). The parts go through NASA Level 1 or ESA Class 1 screening flow and can be brought up to full Level 1 conformance with extra qualification testing if desired. Typical applications include battery management, dc-dc converters, and space motor drives.

Two 100 V parts are available with both bottom-side and top-side cooled packaging. One 650 V 30 A GaN-on-Silicon power transistor is available in a bottom-side cooled package. Each device is available with options for EAR99 or European sourcing. Teledyne e2v HiRel's GaN HEMTs feature single wafer lot traceability, extended temperature performance from -55 to +125°C, and low inductance, low thermal resistance packaging.

www.teledynedefenseelectronics.com

1200V Hermetically Sealed Silicon Carbide Half-Bridge Power Module

Solitron Devices introduced the SD11487, a hermetically sealed SiC Power Module for high reliability applications. With a hermetic packaging format, the 51mm x 30mm x 8mm outline is claimed to be the smallest hermetically sealed high reliability, high voltage, half-bridge on the market. The integrated format maximizes power density while minimizing loop inductance. 60mil pins for the power output stage are isolated on one side of the package to allow simple power bussing while 30mil pins are on the opposite side for control signals.

The SD11487 is a half bridge configuration with two 1200V 12mΩ SiC MOSFETs. Also included in the module are two freewheeling 1200V SiC Schottky diodes in parallel with the MOSFETs and an integrated NTC temperature sensor. Continuous drain current is specified at 95A.

With operating temperatures of -55°C to 175°C, the SD11487 is designed for the most demanding applications such as down hole exploration; space; and avionics. The hermetically sealed copper package combined with the Alumina Nitride direct bond copper substrate provide excellent thermal conductivity as well as case isolation. The integrated temperature sensing enables high level temperature protection.

www.solitrondevices.com

AC/DC Power Supplies for Industrial, IoT, and EV Applications

CUI announced the addition of three, chassis mount AC/DC power supplies housed in compact metal cases with the VGS-500, VGS-350D, and VGS-200E series line of products. The ultra-slim designs make the power supplies appropriate for industrial and IoT use in harsh environments for inductive load applications such as motors, relays, and contactors. The power supplies are also well suited for the growing deployment of electric vehicle charges.

With universal input voltage 85-305VAC or 120-430VDC and a operating temperature (-40 C to +85 C), the products from CUI.

The VGS-200E also has a better MTBF rating over competing products, up to 300,000 hours. All products feature bottom and side installation and are certified to the EN 62368 safety standard with an operating altitude of up to 5,000m.

www.cui.com

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160 V 2-Channel Gate Driver ICs for Battery-Powered Applications

Infineon Technologies announced the expansion of its MOTIX™ family of products for automotive and industrial motor control applications. To further expand the advanced product family, Infineon introduces the 2-channel MOTIX gate driver ICs 2ED2742S01G, 2ED2732S01G, 2ED2748S01G, and 2ED2738S01G. The 160 V Silicon-on-Insulator (SOI) gate drivers are small, powerful, and cost-

effective gate drive solutions with latch-up immunity. They are designed for battery powered applications, including cordless power tools, multicopters, drones, and light electric vehicles with batteries up to 120V.

Infineon's SOI technology eliminates the parasitic thyristor structure and provides excellent robustness and immunity to negative transient voltages at the VS pin. The 2-channel gate drivers have integrated monolithic bootstrap diodes that supply the high-side bootstrap capacitor externally, further reducing system-level BOM costs. The devices come in a compact 3 x 3mm² VSON10 package and are available in both half-bridge (HB) and high-side + low-side (HS + LS) configurations as well as two different source/sink currents to drive n-channel MOSFETs in various applications.

The 2ED2732S01G and the 2ED2742S01G deliver a source current of 1A and a sink current of 2A, while the 2ED2738S01G and the 2ED2748S01G deliver a source current of 4A and a sink current of 8A. All products feature independent undervoltage lockout (UVLO) on both VCC and VB pins – the HB products also integrate shoot-through protection (STP). In addition, the MOTIX 160 V solutions are fully qualified for industrial applications according to the relevant JEDEC78/20/22 tests.

www.infineon.com

HEMT Family in Easy-to-Use Flip Chip QFN Packaging

Innoscience Technology has announced a range of low voltage discrete HEMTs in FCQFN packaging. Rated at 40 V, 100 V and 150 V, the 'flip chip' formatting makes it simple for engineers to use.

40 V-rated FCQFN devices are available with an on-resistance value of 4.3mΩ (3x4mm^2 chip size). 100 V HEMTs are offered with $R_{DS(on)}$ ratings of 2.8mΩ (3x5mm^2) and 1.8mΩ (4x6mm^2), while the 150 V-rated parts measuring 4x6mm^2 are available with 3.9mΩ and 7 mΩ $R_{DS(on)}$.

The 40 V parts using Innoscience's latest GaN processes achieve performance with figure-of-merit (FOM) values for Q_{gg}*R_{on} and I_{dss}*R_{on}. The parts low drain and gate leakage currents enable them to be used in mobile markets and direct-battery-connected applications. Other applications include USB Type C buck-boost converters in laptops. Furthermore, with its latest generation process, Innoscience maintains very tight control of the epitaxy, resulting in a very uniform threshold voltage and on-resistance, leading to a very high wafer yield.

100V devices suit DC/DC conversion at power levels of up to 2kW, due to their very low on-resistance. When used in parallel configuration, power levels up to 8kW can be achieved.

The 150V targets industrial applications, including solar installations. They have been designed to be very rugged so they do not need the industry-standard 80% derating to be applied (i.e. they are rated at 100% of their voltage). All the 40V, 100V and 150V HEMTs have been tested to and exceeded JEDEC and the GaN-specific JEP 180 standards.

www.innoscience.com

Motor Driver ICs Enable Full Torque at Zero Speed for Sensorless BLDC Motors

Renesas Electronics introduced a family of motor driver ICs for brushless DC (BLDC) motor applications. The devices implement Renesas' patent-pending technologies that enable full torque at zero speed from motors without sensors. The motor driver ICs enable Renesas customers to design sensorless BLDC motor systems with higher horsepower and speed at a given torque. They also improve power consumption and reliability, while reducing cost and board space by lowering the number of components designers need to use.

Renesas is introducing three motor driver ICs with the new technology: RAA306012 65V is a standalone 3-phase Smart Driver device that can be paired with a variety of MCUs from Renesas or from other sources. The RAJ306101 integrates a Renesas RX13T 32-bit MCU with the RAA306012 in a single package, reducing board space and improving cost and reliability. The RAJ306102 integrates a 16-bit Renesas RL78/G1F MCU with the RAA306012, providing similar integration benefits.

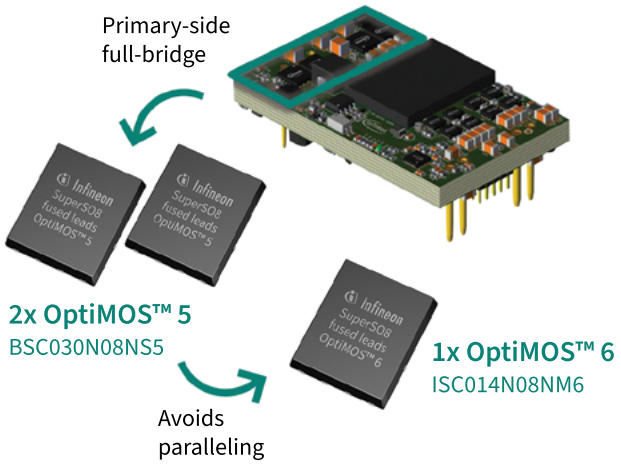
www.renesas.com

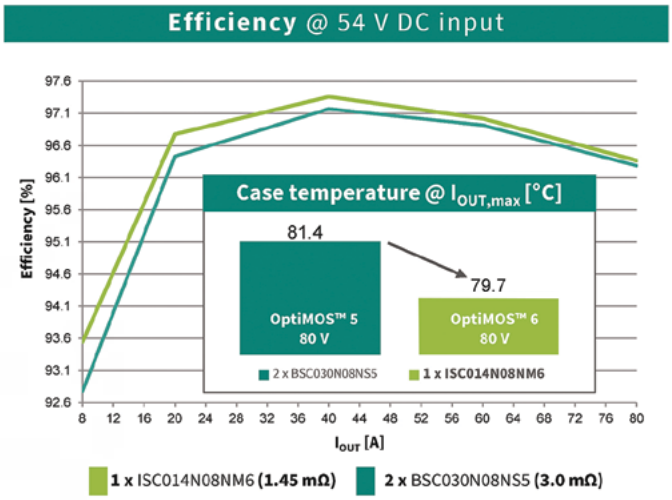
Advertising Index

The value proposition of OptiMOS™ 6 80 V power MOSFET has been clearly demonstrated in application tests

Datacom soft-switching LLC 1 kW ¼ brick application

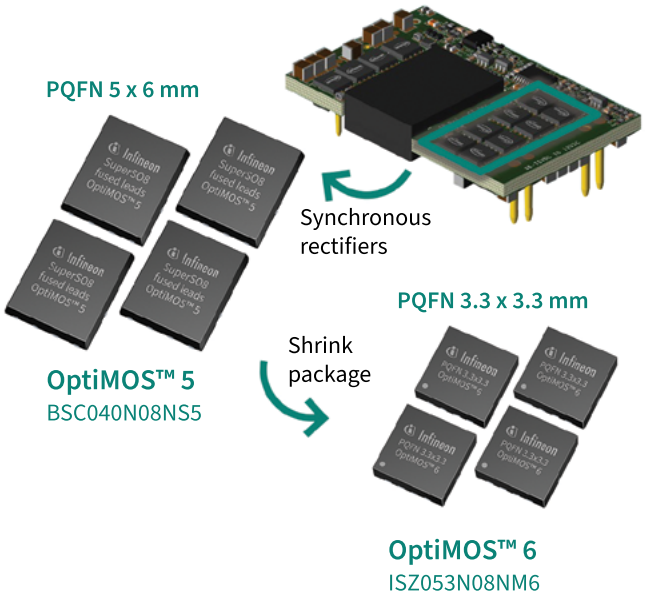
OptiMOS™ 6 80 V ISC014N08NM6 (1.45 mΩ) with the industry's lowest $R_{DS(on)}$ in a SuperSO8 package (PQFN 5 x 6 mm) replaces two OptiMOS™ 5 BSC030N08NS5 (3.0 mΩ). The efficiency also improves by up to 0.8 percent, thanks to improvements in Q_g, Q_{gd}, and R_{oss}.

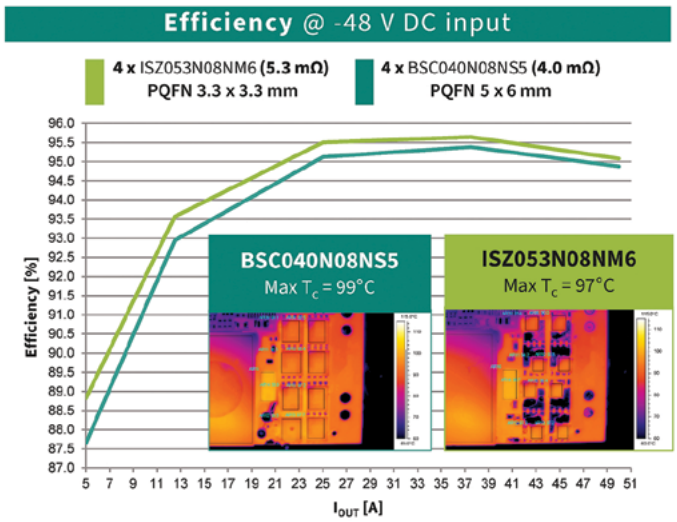




Telecom hard-switching full-bridge/center-tap, 600 W ¼ brick application

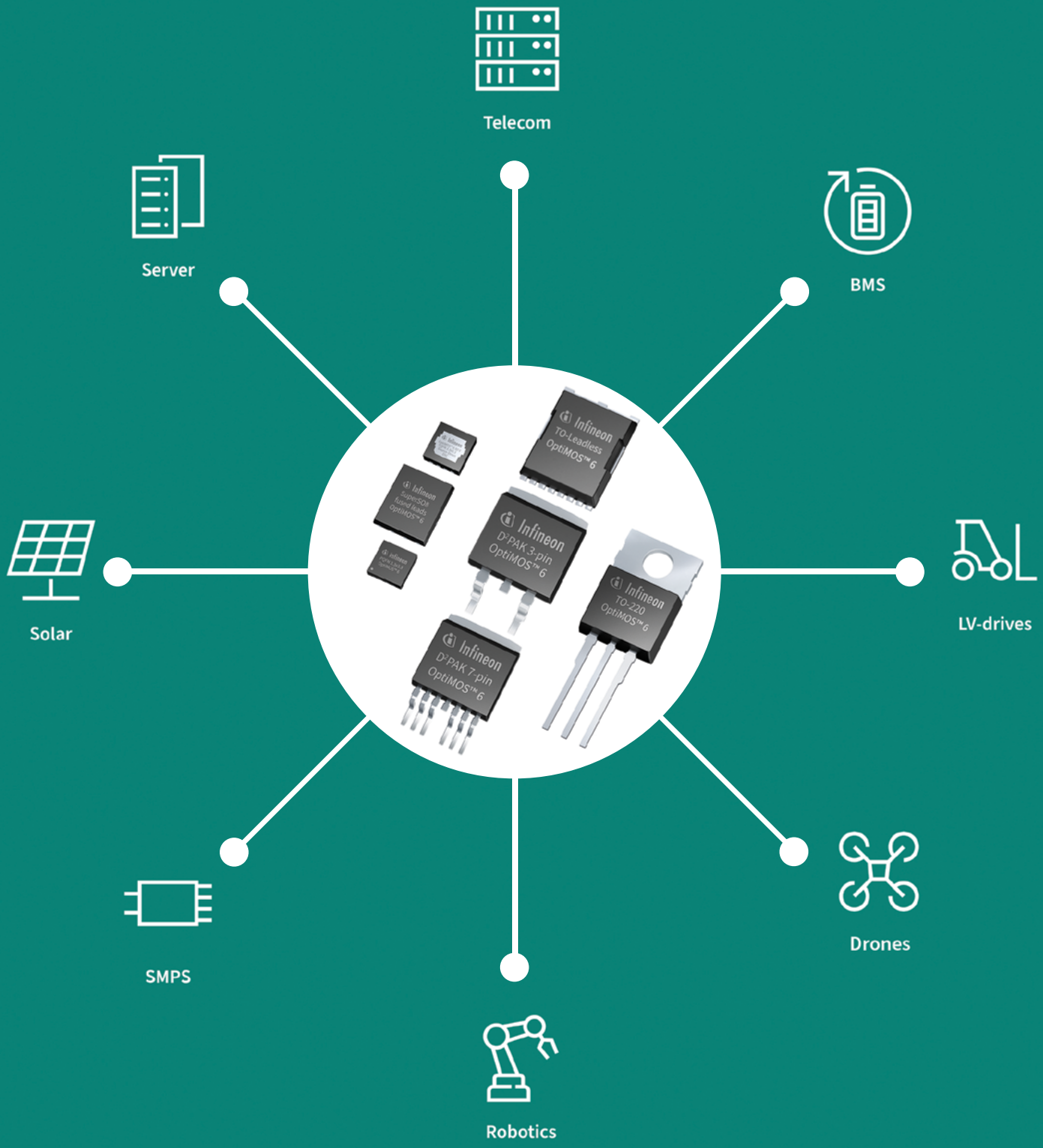
OptiMOS™ 6 80 V ISZ053N08NM6 (5.3 mΩ) with the industry's lowest $R_{DS(on)}$ in a PQFN 3.3 x 3.3 mm package enables compact designs with 64 percent PCB area reduction. Mid- to full-load efficiency also improves by up to 0.3 percent, thanks to lower Q_{oss} and improvement in figures of merit and Q_{rr}.





For more details scan the QR code.

Bring your design to the next level of system efficiency with OptiMOS™ 6 power MOSFETs



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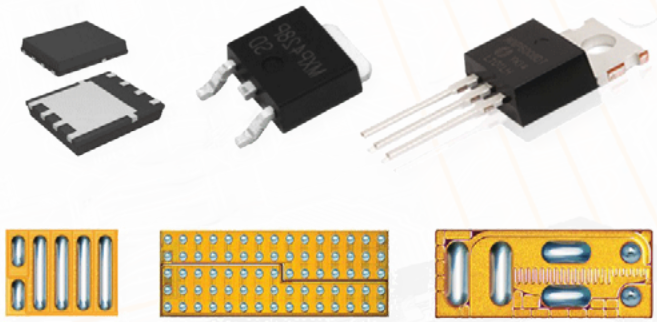

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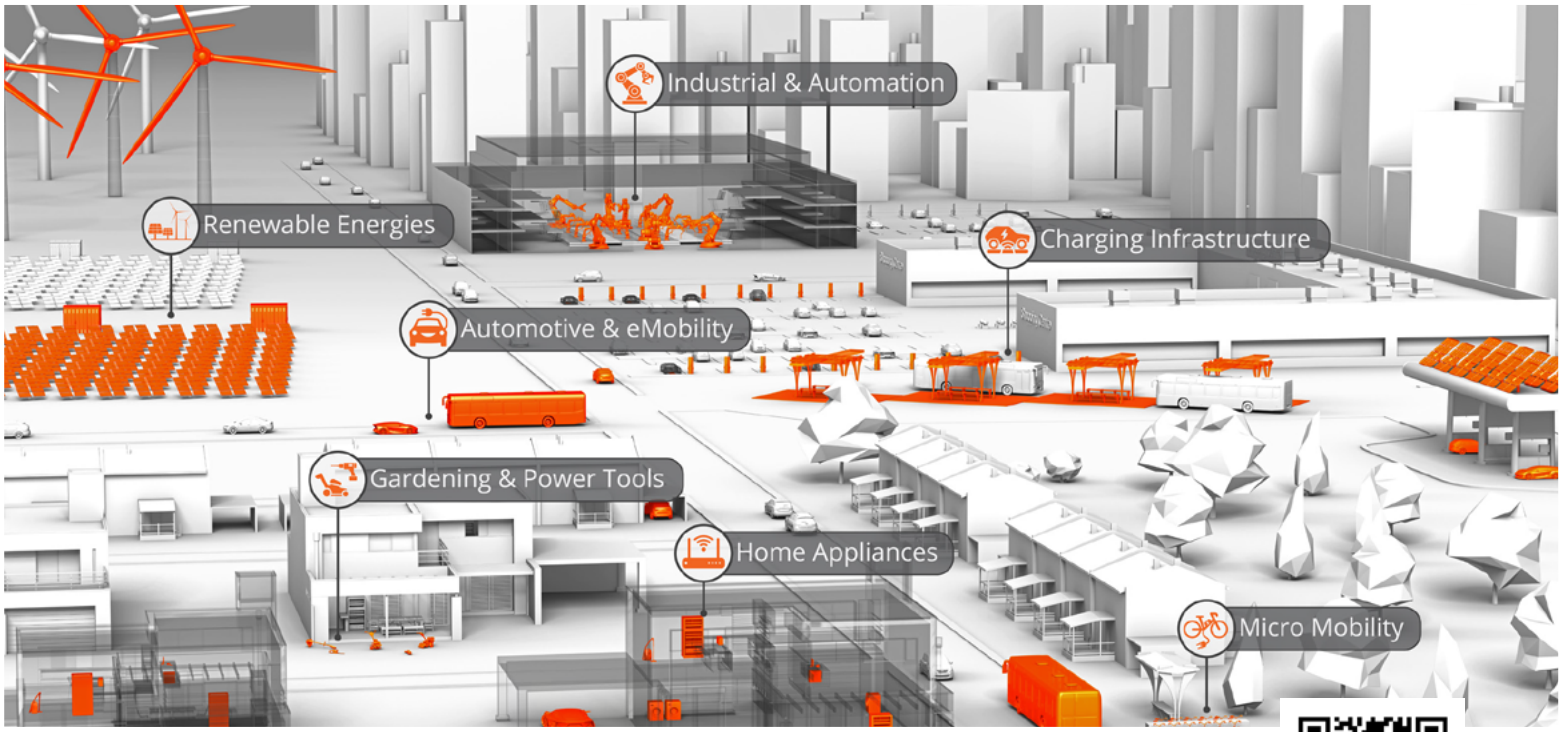

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